# *Advanced Issues in HEMT Simulation*

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# Contents

- Piezoelectric charge, nucleation layer and semi-insulating traps in GaN / AlGaN HEMT
- Hot Carrier Trapping in GaN / AlGaN HEMT
- impact ionization effect in InGaAs HEMT

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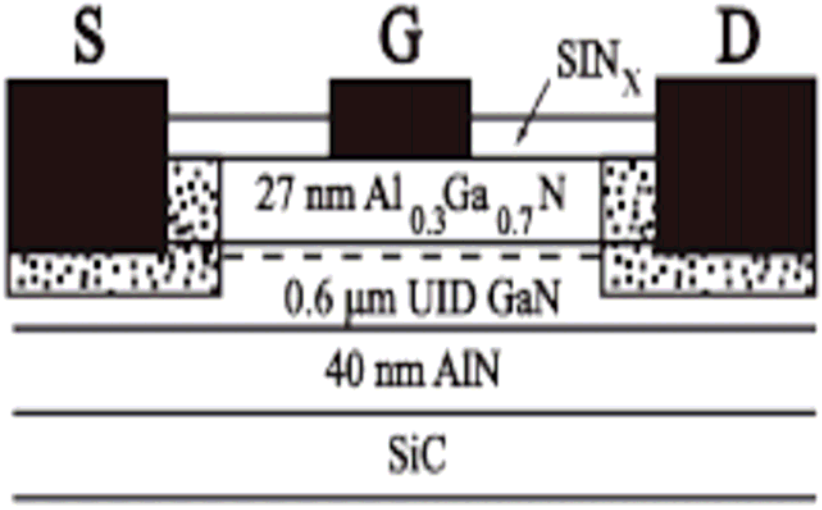
# Introduction

- Wide bandgap and polarization nature of InGaN and GaN of HEMTs contributing to a high sheet charge density in the 2-dimensional electron gas (2-DEG).
- Strain-induced piezoelectric polarization and the spontaneous polarization directly affect performances of various HEMT structures.
- Use of Aluminum nitride (AlN) nucleation layer and/or semi-insulating substrate traps in the HEMTs suppresses parasitic conduction in the substrate and leads to better pinch-off condition.
- APSYS simulator offers accurate simulation capability in wide bandgap nitride-based HEMTs.

# HEMT schematic layer structure

- 2-D conduction n-channel formed at the AlGaN/GaN heterointerface.

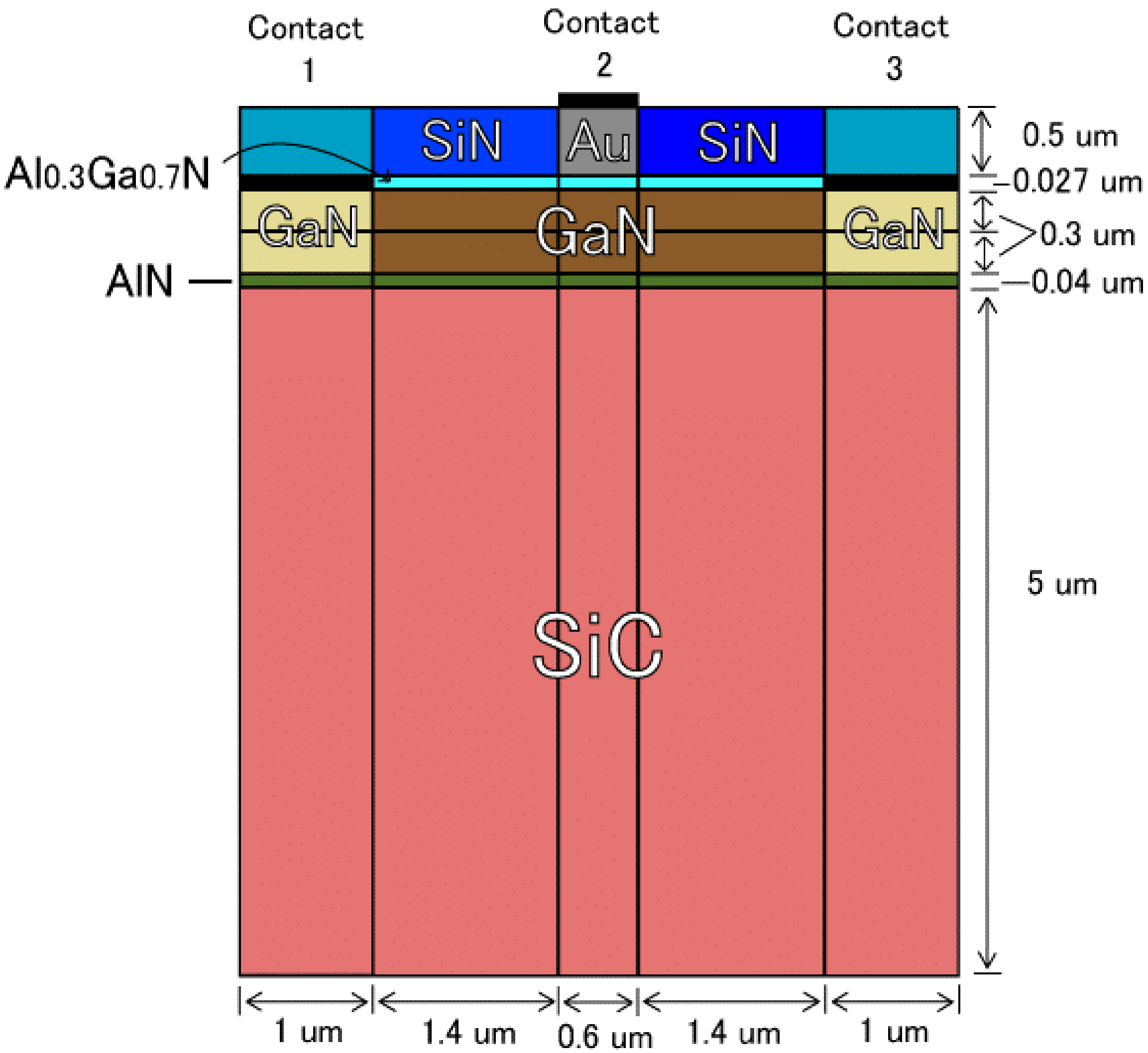



Ref: F. Recht et. al., "Nonalloyed ohmic contacts in AlGaN/GaN HEMTs by ion implantation with reduced activation annealing temperature," IEEE Elec. Dev. Lett., vol. 27, no. 4, April 2006, pp. 205-207

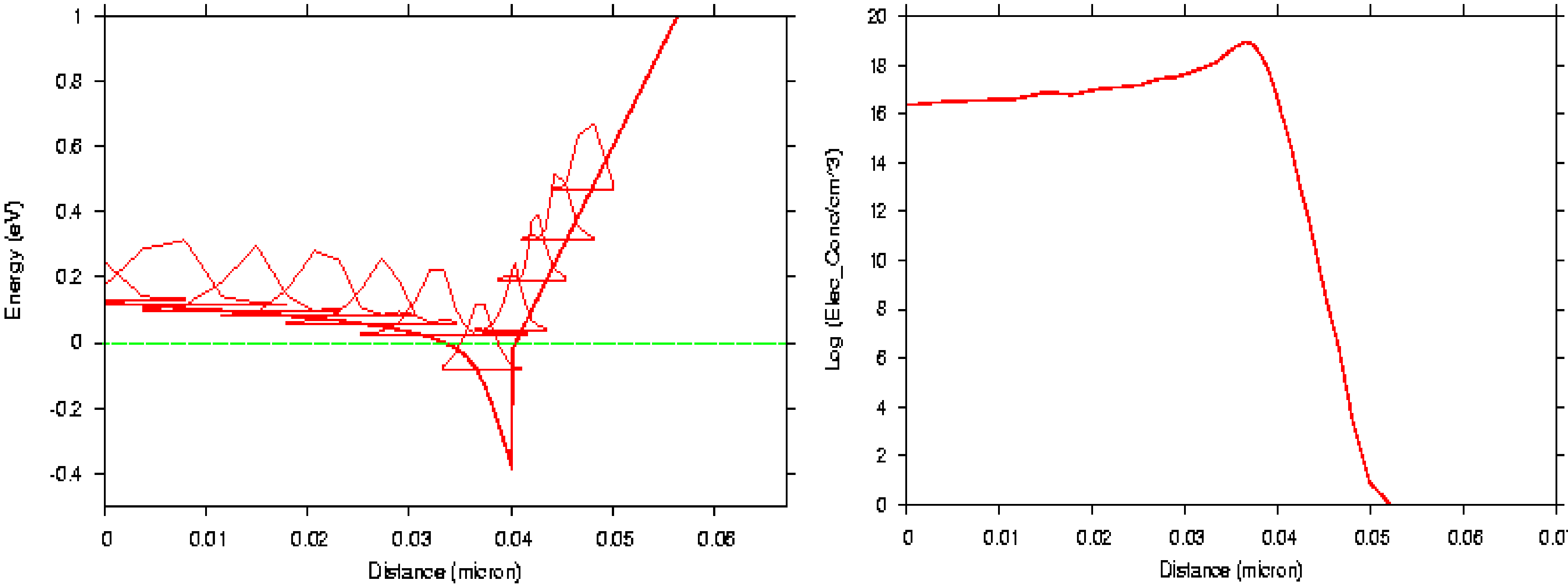
# Setup of layer file with Layerbuilder

- Piezoelectric surface charge is defined and its value at the AlGaN/GaN heterointerface.
- Semi-insulating substrate traps are defined in the SiC substrate.
- Contact 1: Source (Ohmic)
  Contact 2: Drain (Ohmic)
  Contact 3: Gate (Schottky*)

*proper metal (Au) work function is used.



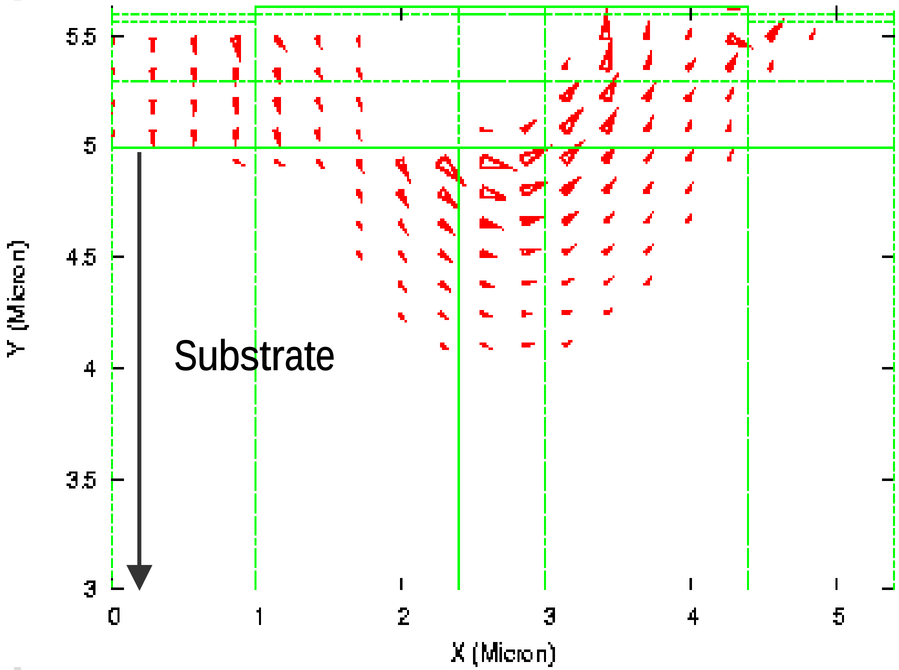
# Quantum confinement effect

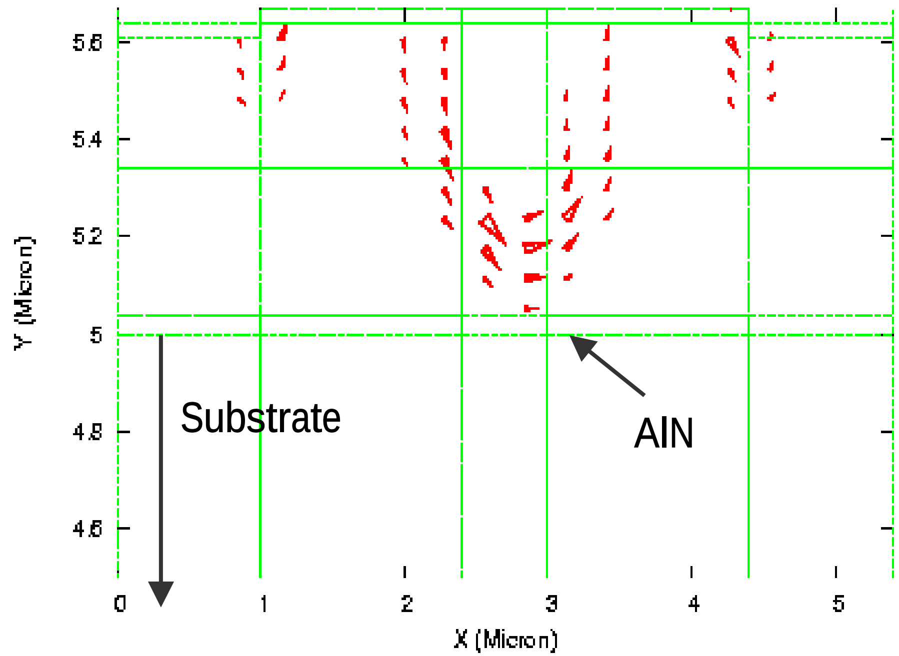



Left:: Band diagram and corresponding quantum subband states with wave functions at equilibrium are shown.

Right: Electron concentration at equilibrium near the 2-DEG is shown.

# Electron flow at Pinch-off

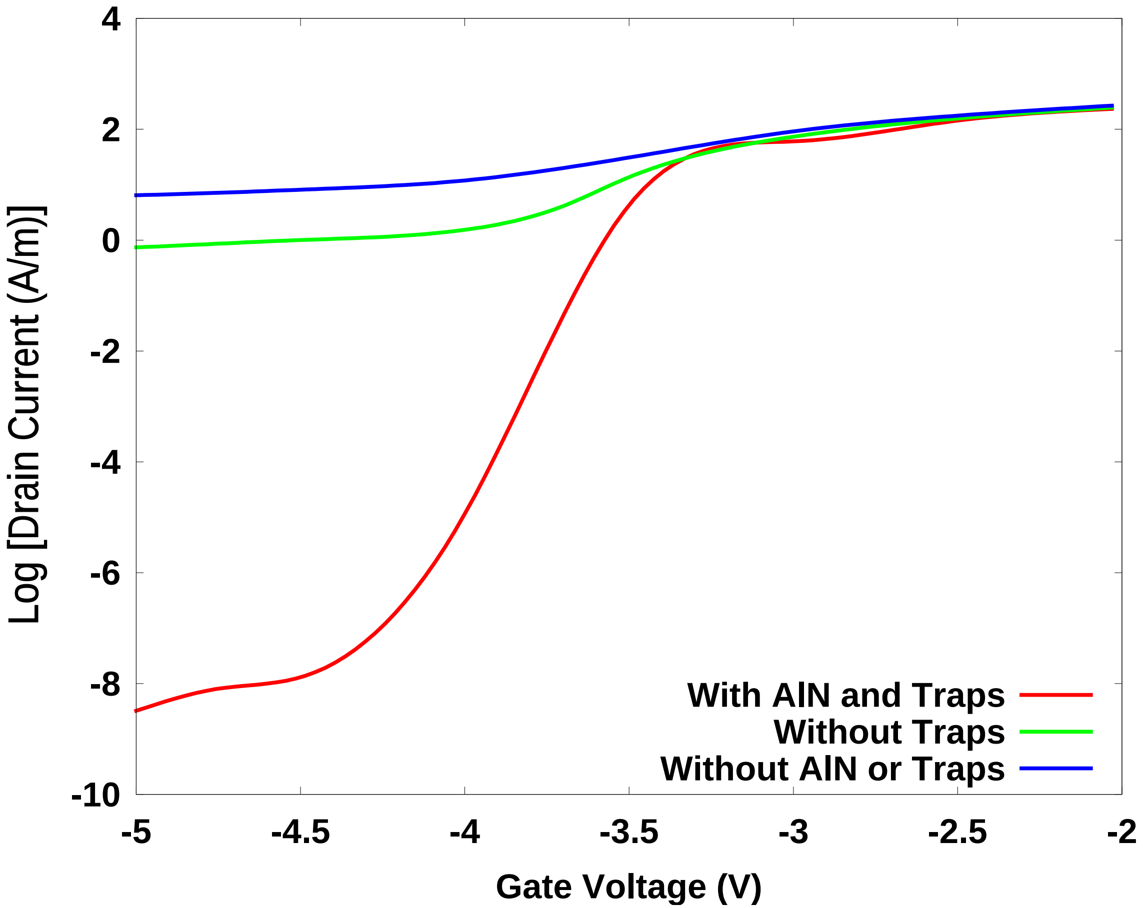



Left:: electrons spill over into the substrate at pinch-off in the *absence* of both the AlN layer and the semi-insulating substrate traps, introducing parasitic current in the substrate.

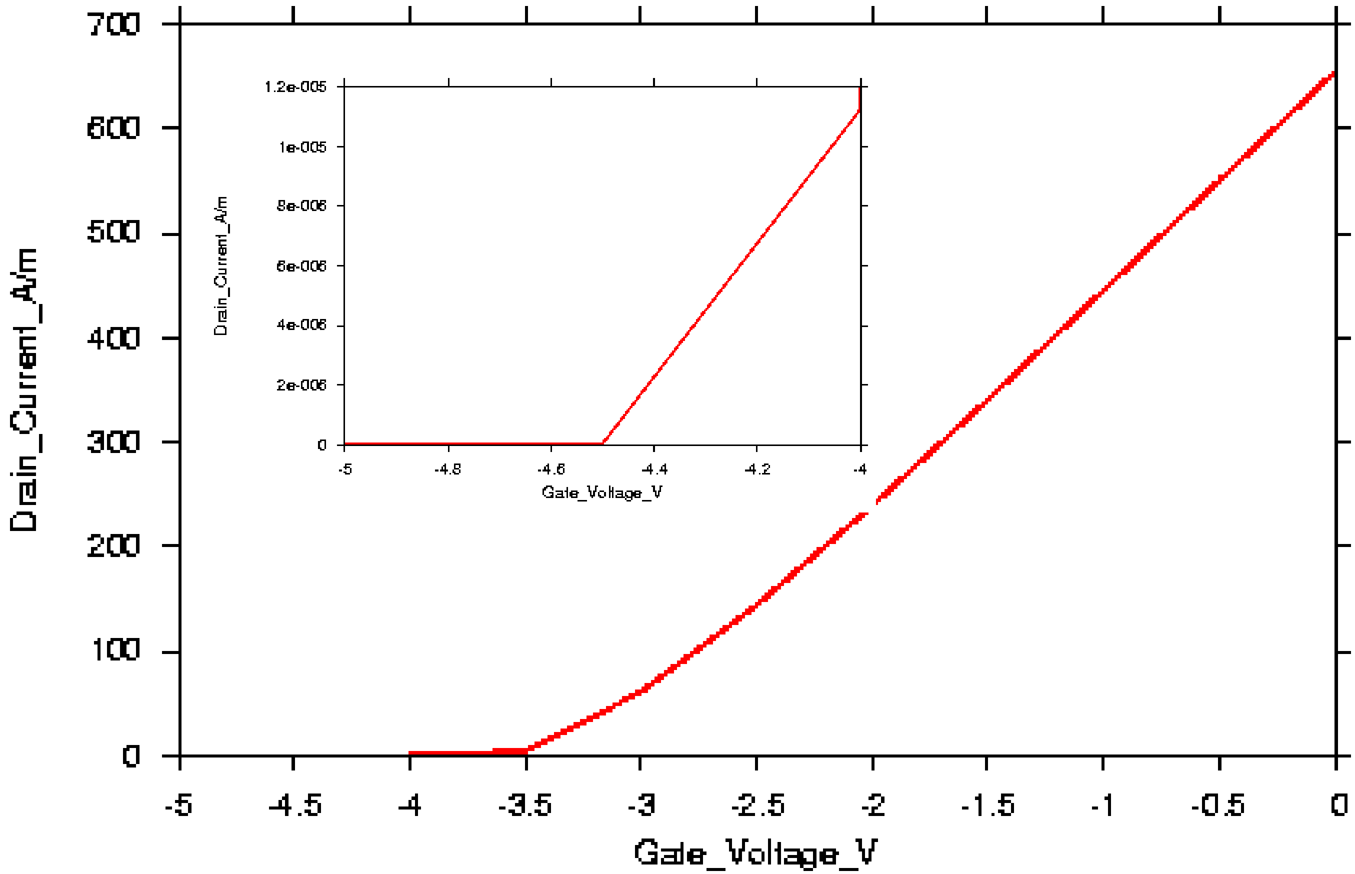
Right: electrons are “kept” well within the GaN buffer at pinch-off in the *presence* of both the AlN layer and the semi-insulating substrate traps, suppressing the parasitic current in the substrate.

# Threshold current behavior




Results show pinch-off behavior strongly dependent on AlN and trapping in the substrate

# Simulated Id-Vg




In the optimized simulation (with both the AlN layer and the substrate semi-insulating traps), the drain current vs. gate voltage plot shows the pinch-off voltage at ~ -4.5 V, matching the experimental data. (The leakage drain current is in the order of 10^-6 A/m at 4.5 V, as shown in the inset)

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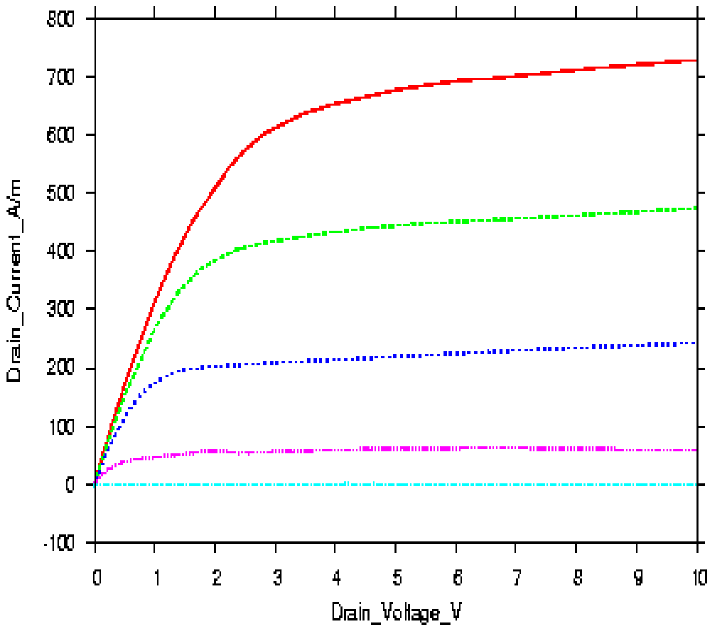
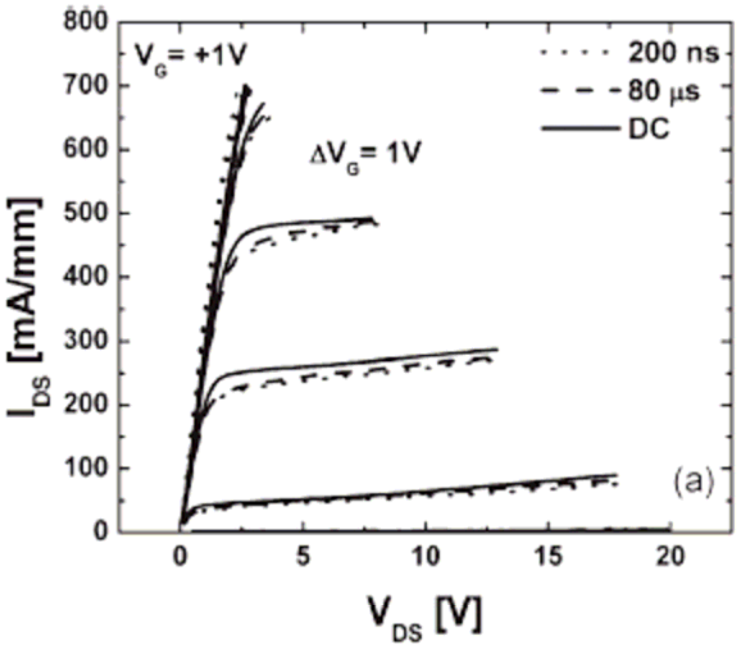
# Drain current-voltage characteristics




Left: : Simulated drain current-voltage output characteristics with the gate voltage varying from 0 to -4 V in steps of 1 V (downward).

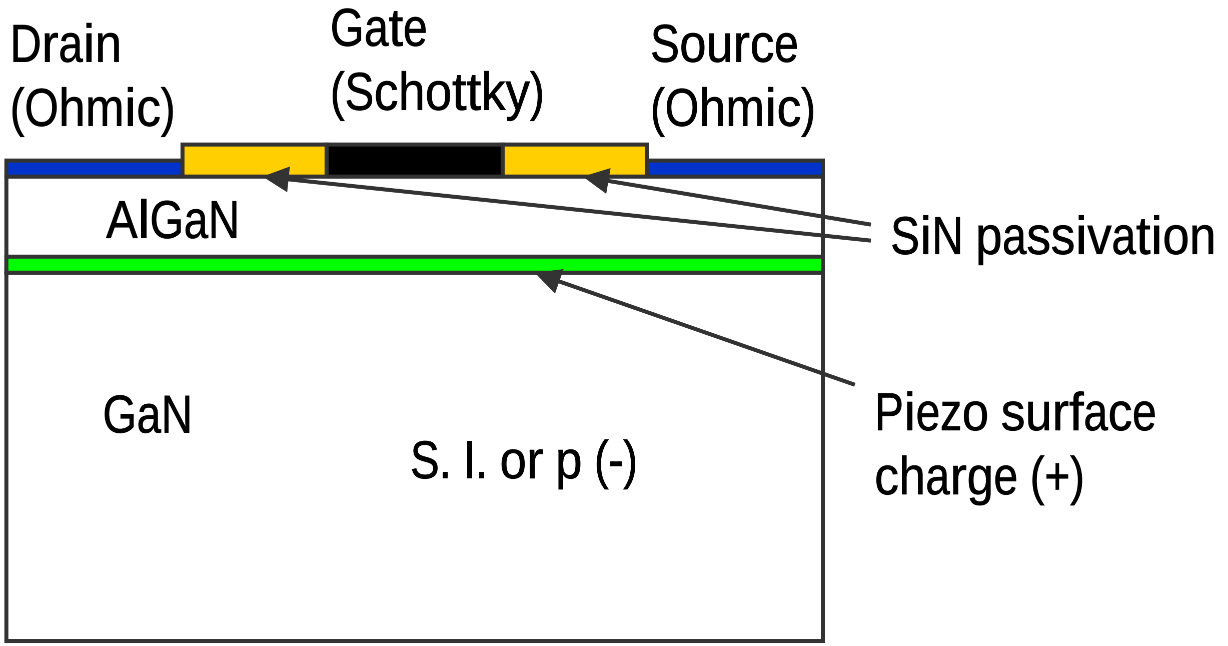
Right: Experimental drain current-voltage output characteristics.

# Summary

- Piezoelectric surface charge has been found to be critical for the formation of the 2-DEG conduction channel.
- Aluminum nitride (AlN) nucleation layer and the substrate semi-insulating traps are effective in suppression of substrate parasitic conduction.
- Reasonable agreement between simulated and experimental measurement results have been obtained.

# Contents

# Basic Structure




- Substrate should be semi-insulating (S.I.) or p (-) in order to confine the n-channel. ( Ref: APL Vol. 78, p. 757, 2001)
- SiN passivated AlGaN surface should be described by Fermi-level pinning surface trap states. (Ref:APL vol. 86, p. 42107,2005)

# Hot Carrier Issues

- Realistic model should include interface traps and bulk traps in S.I. GaN substrate.
- Generation of traps by hot carriers may be the source of degradation as seen in silicon MOSFET.
- Trapping of hot carriers also directly affect HEMT performance.
- Proposed simulation studies: comparison of same structure with and without deep level traps; Also with and without hot carrier model.

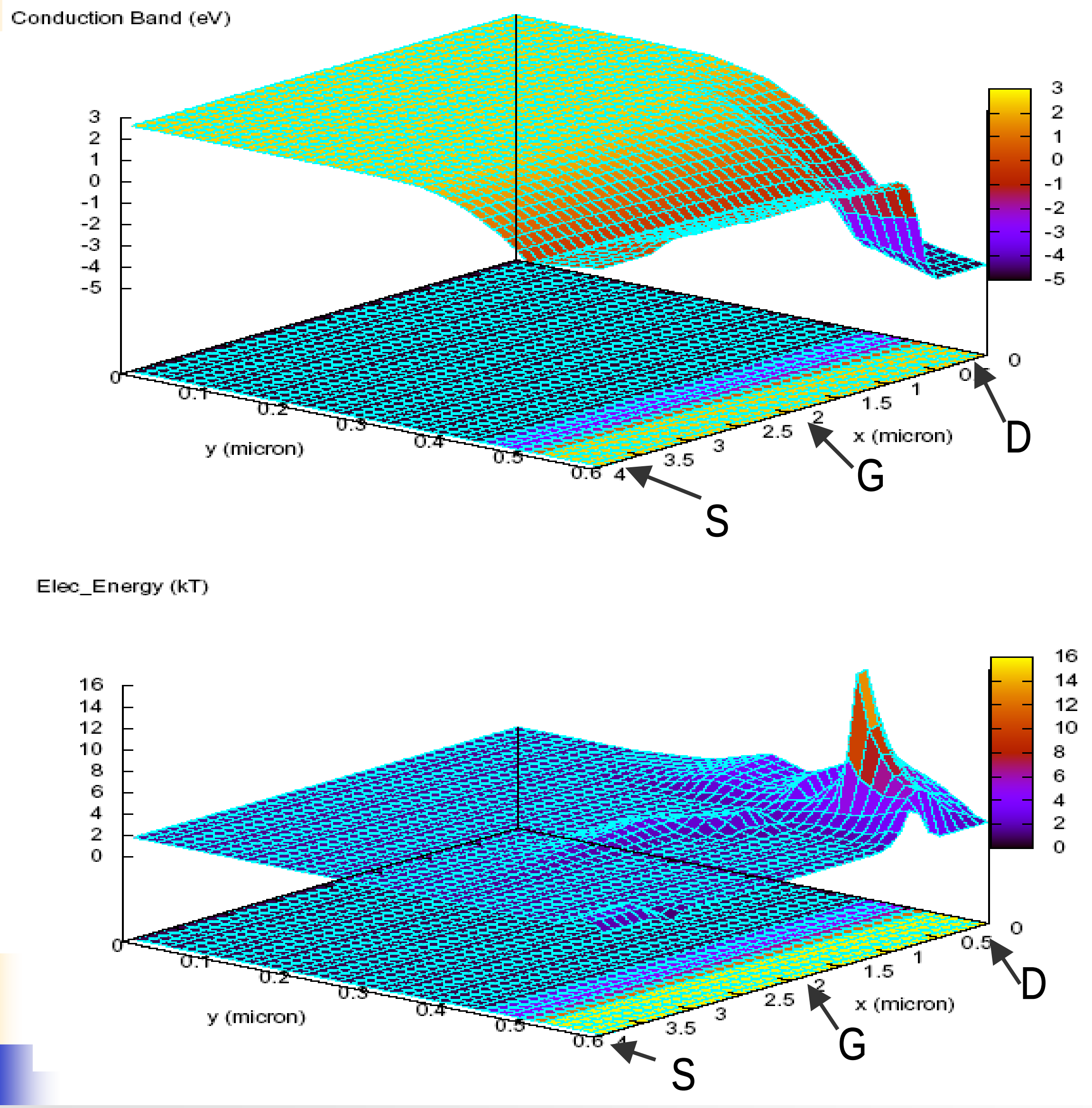
# APSYS Simulator Features

- Hot electron energy distribution modeled by a hydrodynamic equation with carrier energy dependent mobility.
- DC and AC rate equation for deep level traps parameterized by charge types, trap energy levels and capture cross sections.
- Multiple trap models implemented for both bulk and surface.
- Quantum confinement of hot carriers in 2DEG considered.

# Sample Results

(a)

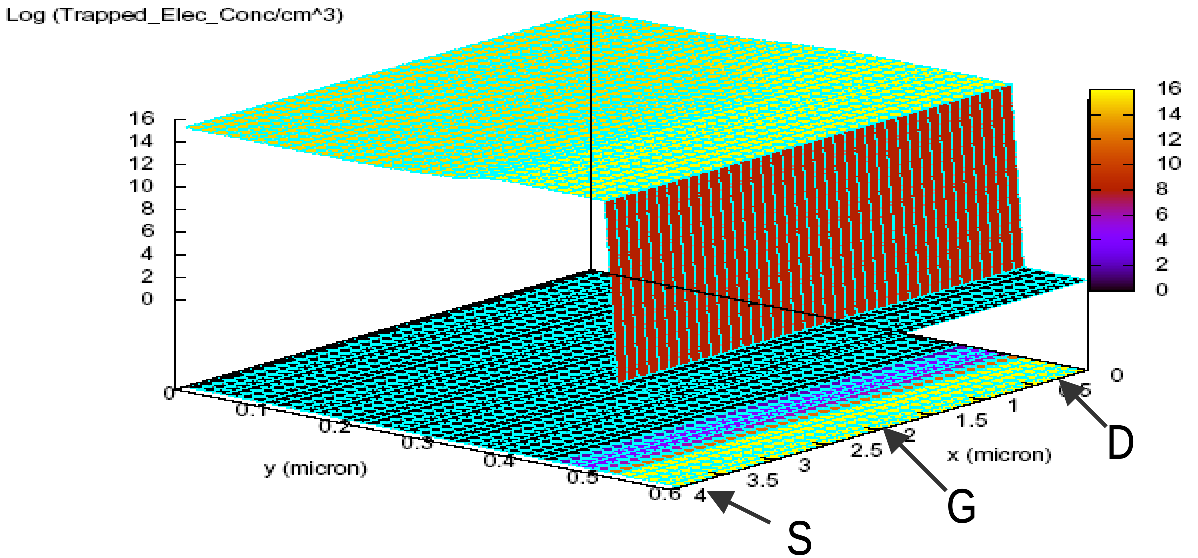
(b)



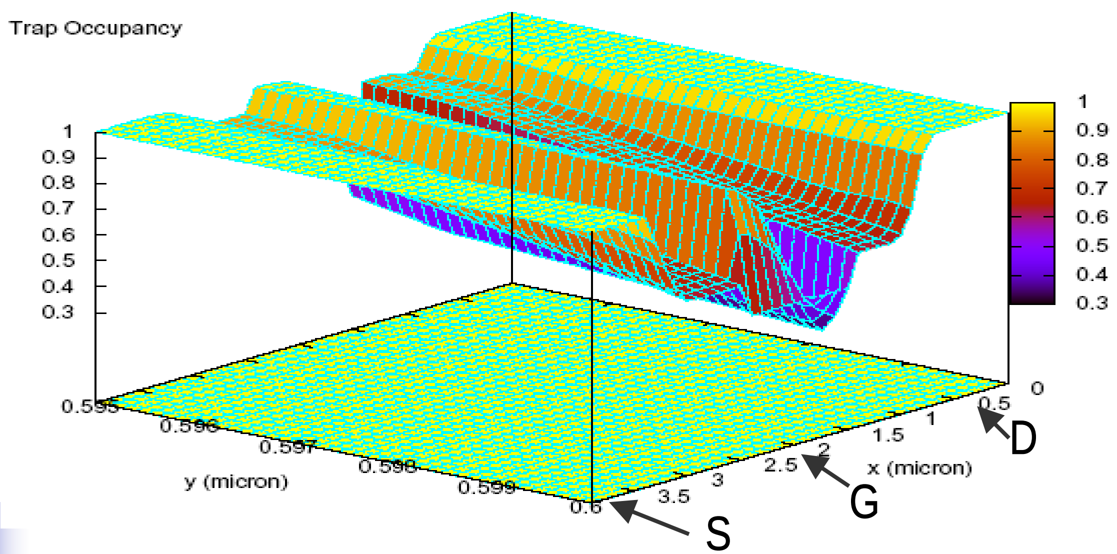

Conduction band profile (a) and electron energy (b) distribution at Vd=5 V and Vg=0.5 V

# Trapped electrons

(a)

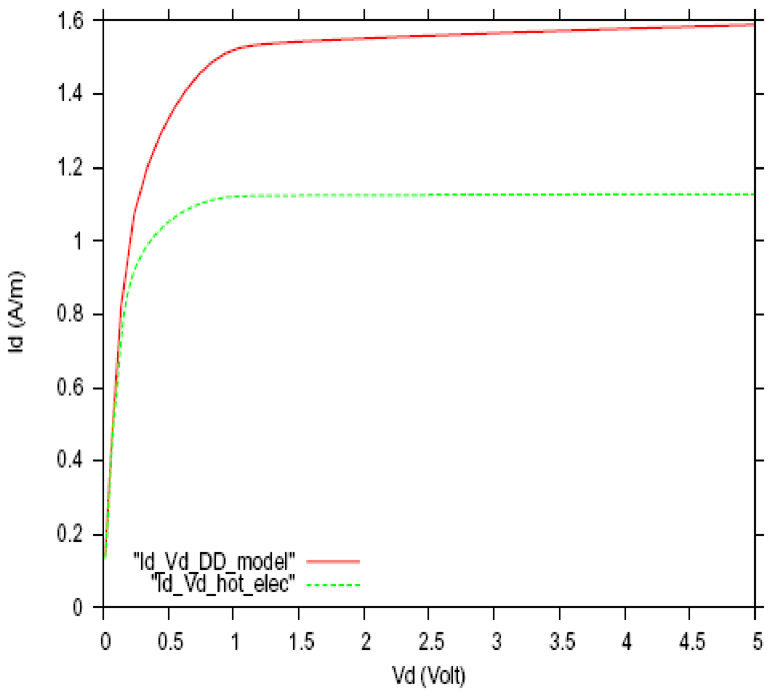


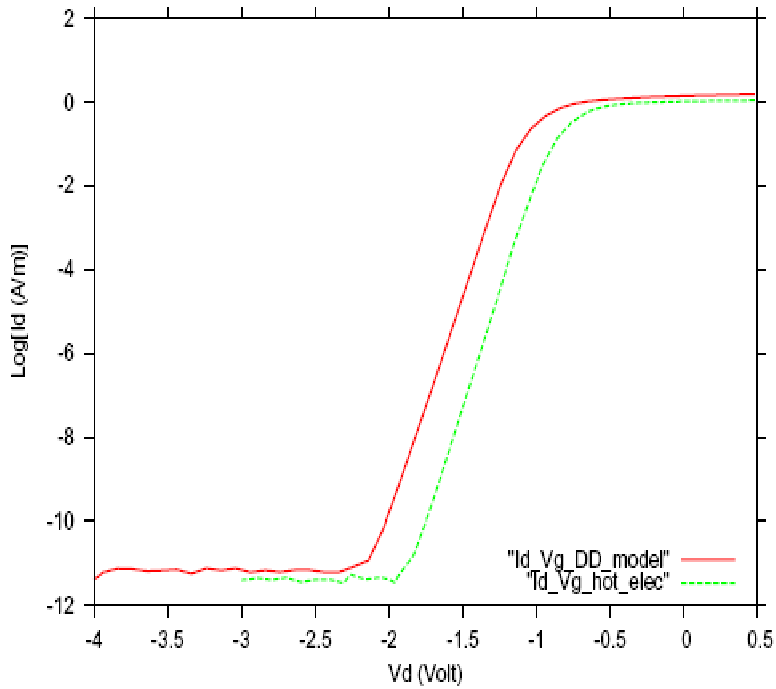

(b)




Trapped bulk electrons at the S.I. substrate (a) and surface trap occupancy (b) distribution at Vd=5 V and Vg=0.5 V

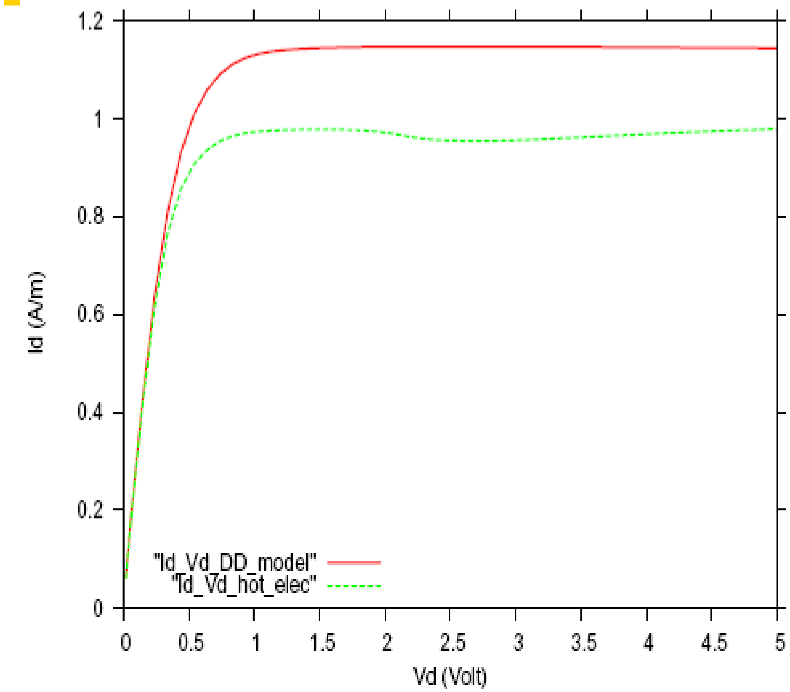
# Drain current characteristics (no traps)

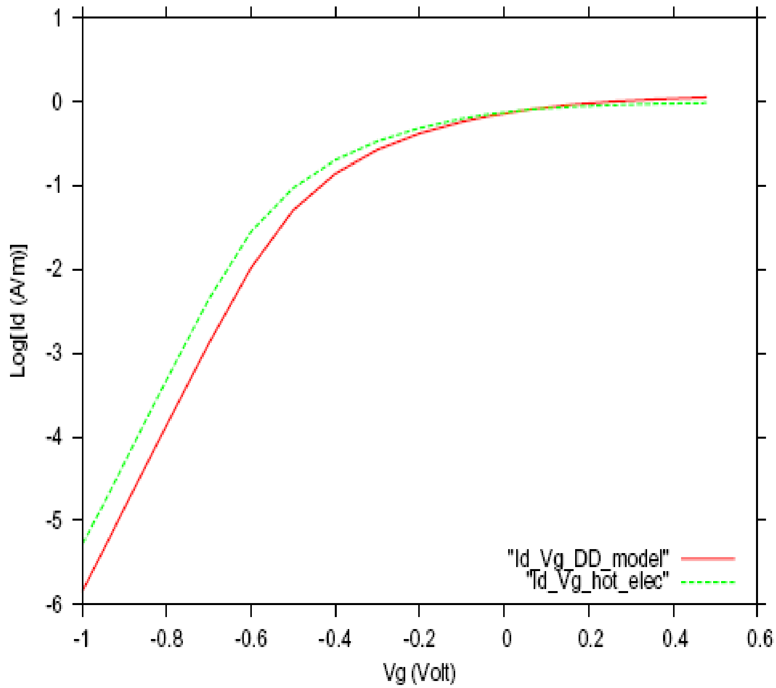



Without deep levels traps, hot carrier model predicts a lower drain current and a positive shift of Vt ➔ no threshold voltage degradation.
Main cause of difference: electron energy dependent mobility model.

# Drain current characteristics (with traps)




With deep levels traps, hot carrier model predicts a lower drain current and a negative shift of Vt ➔ threshold voltage degradation observed, I.e., the FET is more difficult to switch off.
Main cause of degradation: hot electrons overcome potential barriers to be trapped and become harder to be released.

# Summary

- APSYS simulator offers realistic hot carrier degradation modeling with bulk and surface trap distributions.
- Trap distribution determines threshold voltage behavior with or without hot carriers.
- Significant negative shift in Vt due to hot carrier trapping has been observed through numerical simulation with APSYS.

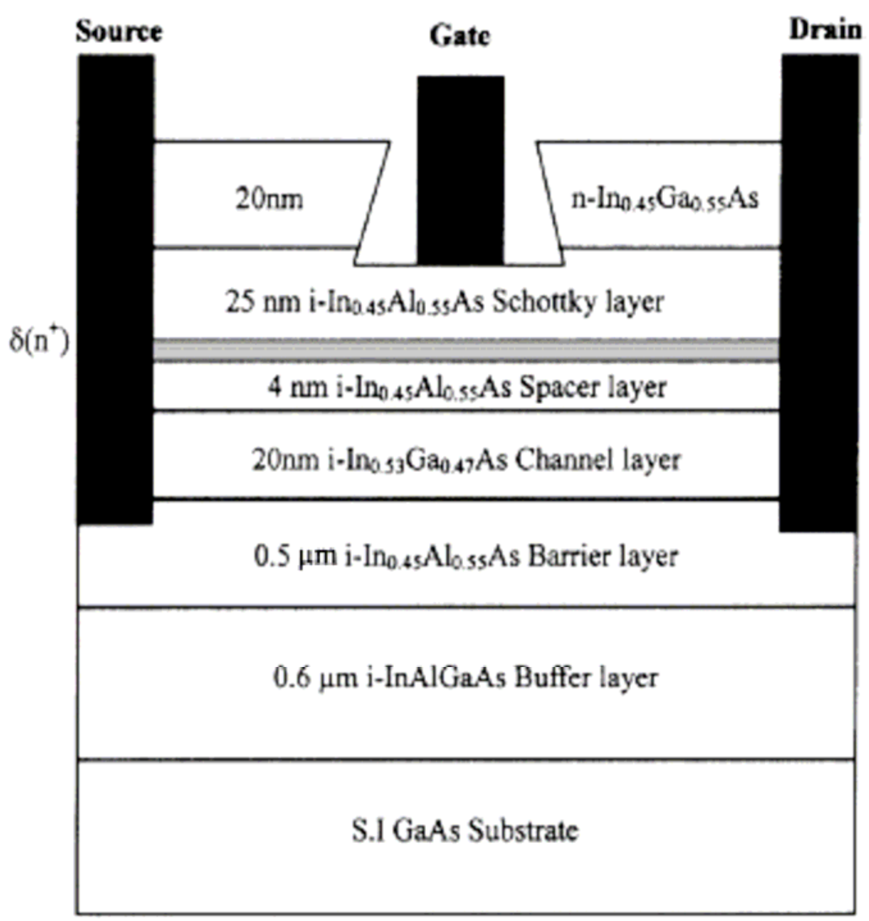
# Contents

# Impact Ionization Effects

- Narrow bandgap HEMT's with InGaAs channel offer high gain and low noise but impact ionization is a major limitation.
- Design issues include gate metal choice and confining barrier band structure engineering.
- APSYS simulator accurately accounts for impact ionization and quantum confinement effects.

# Schematic HEMT layer structure

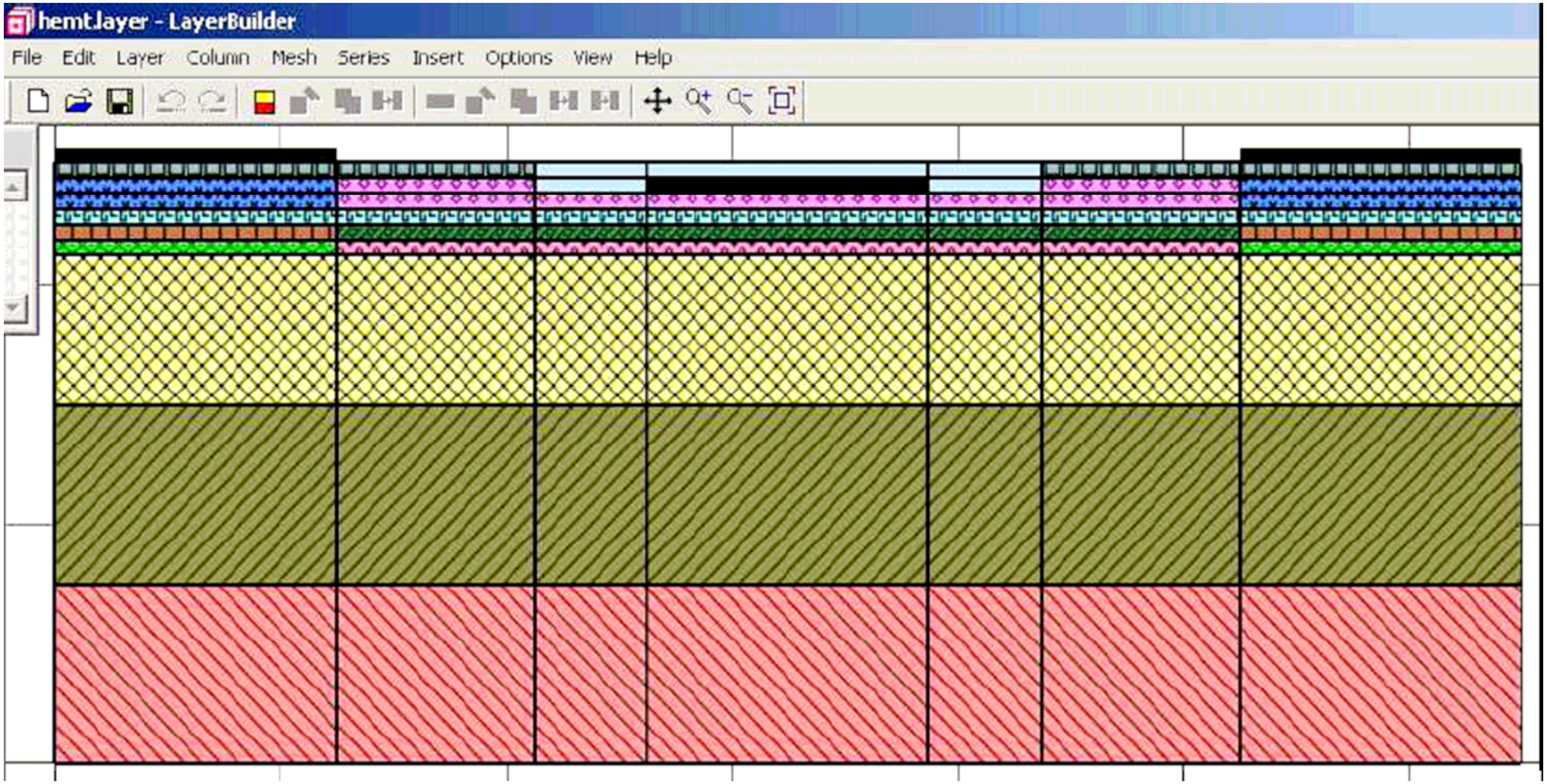
**3-nm planar Si delta-doping $In_{0.45}Al_{0.55}As$ layer**




**Strain expected for 4-nm i-$In_{0.45}Al_{0.55}As$ spacer & 20-nm i-$In_{0.53}Ga_{0.47}As$ channel layers, but strain could be relaxed due to thick growth for 0.5-um i-$In_{0.45}Al_{0.55}As$ barrier layer**

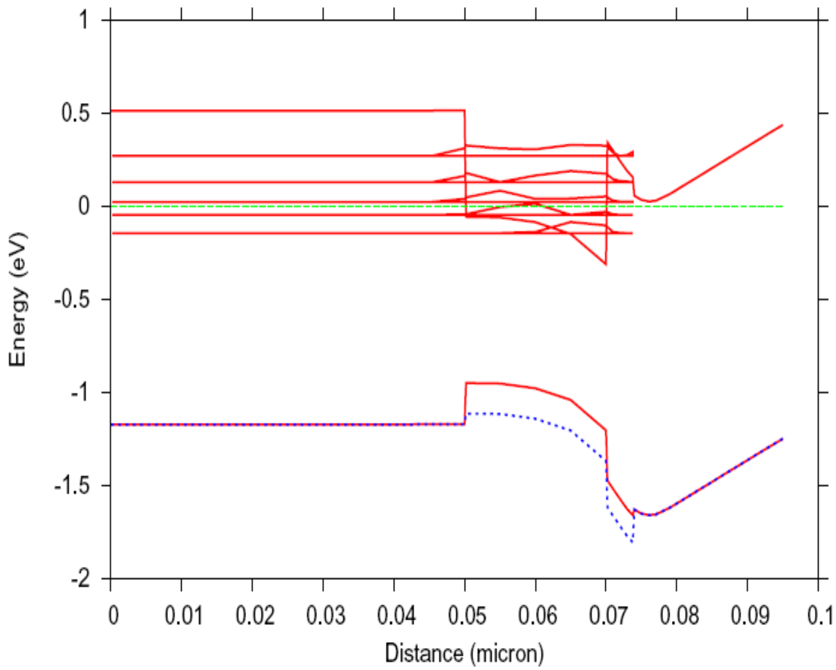
**See: Y J Chen et al, APL Vol 85 No 21 (2004) pp 5087-5089**

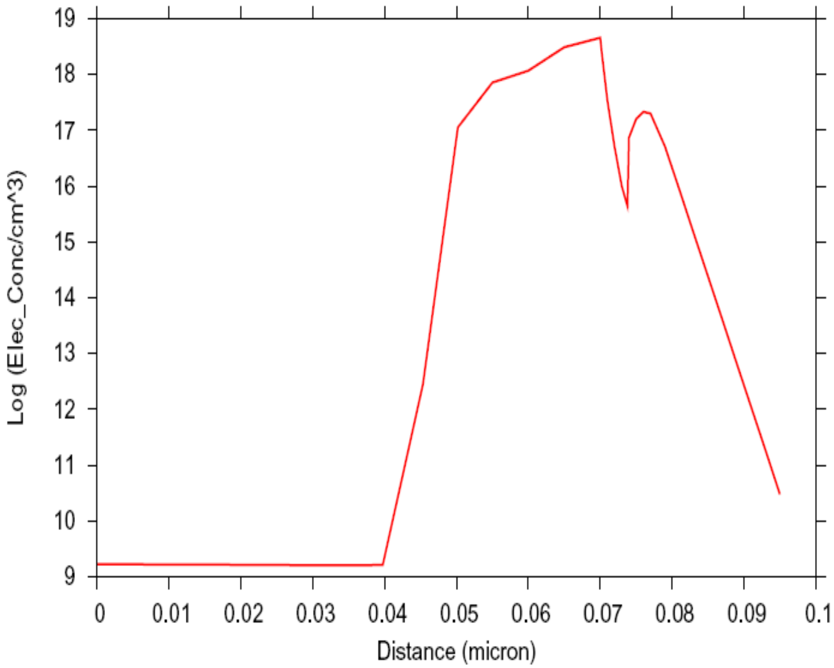
# Setup of layer file with Layerbuilder




**From channel layer upward, the layers under S/D region, i.e. the 1st & 7th columns are heavily doped. Complex layers include three layers: channel & its two neighboring layers.**

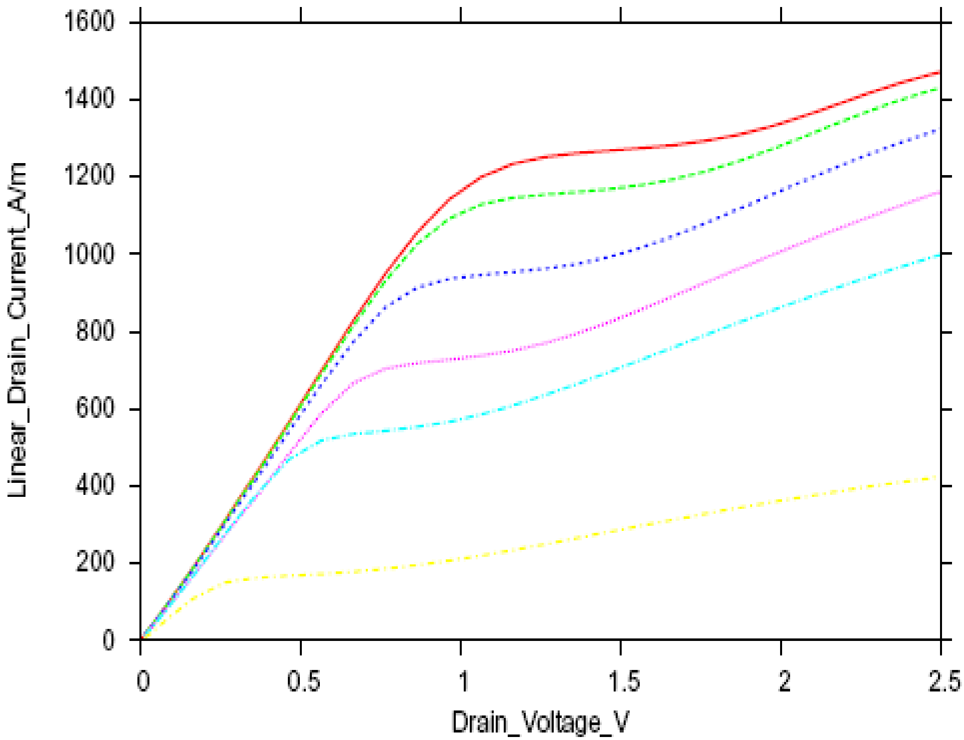
# Quantum Confinement Effect

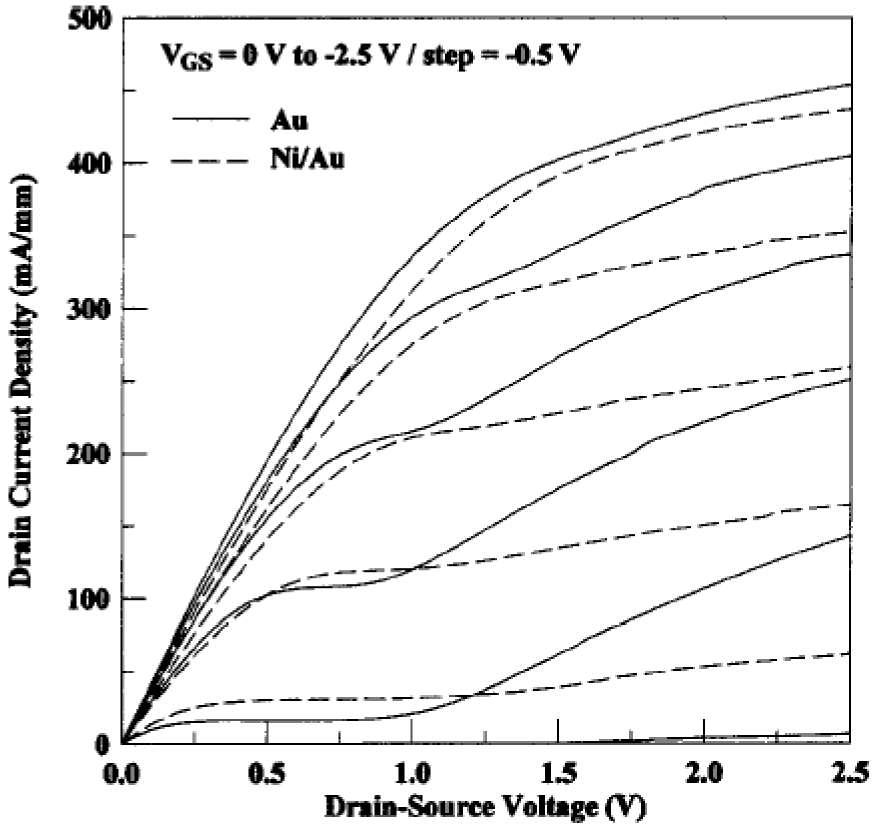



Band diagram and corresponding quantum subband states at equilibrium are indicated on the left.  The electron concentration is shown on the right.

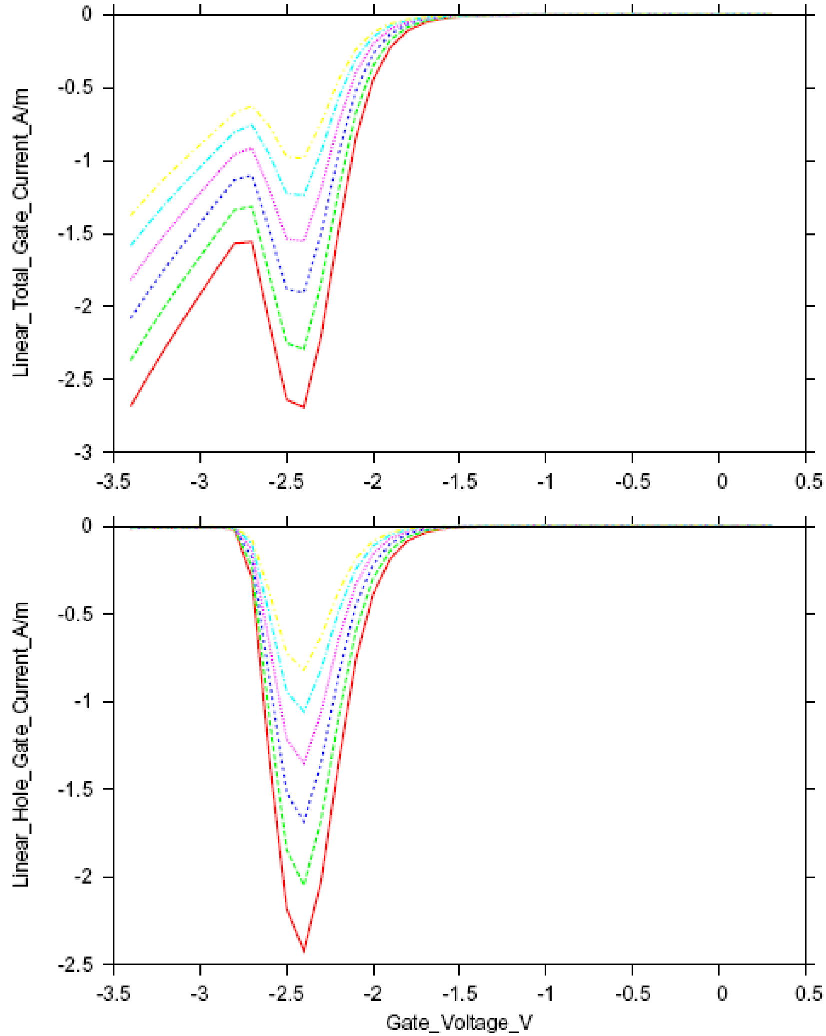
# Kink Effect in Drain Current

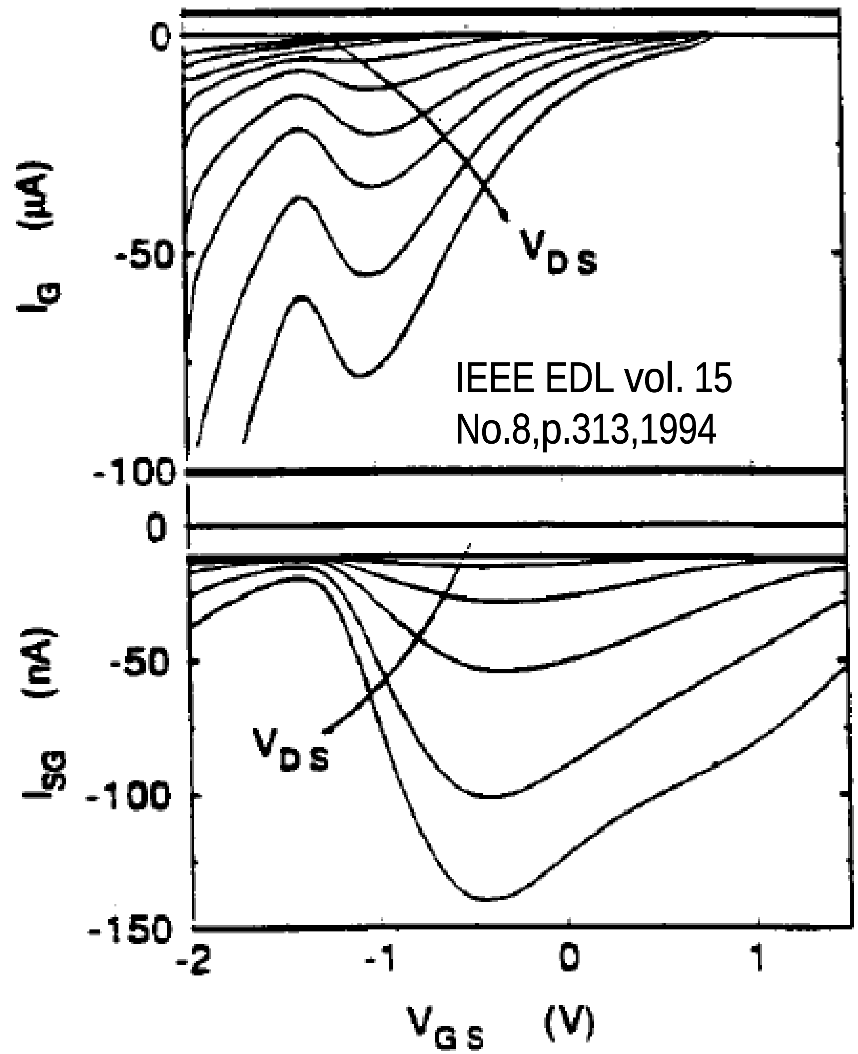



**Ids vs Vds curves (Vgs at 0, -0.5, -1,-1.5,-2 & -2.5 V downward). Notice the kink effect due to impact ionization. Experimental data on the right taken from APL Vol. 85 No. 21, p. 5087, 2004.**

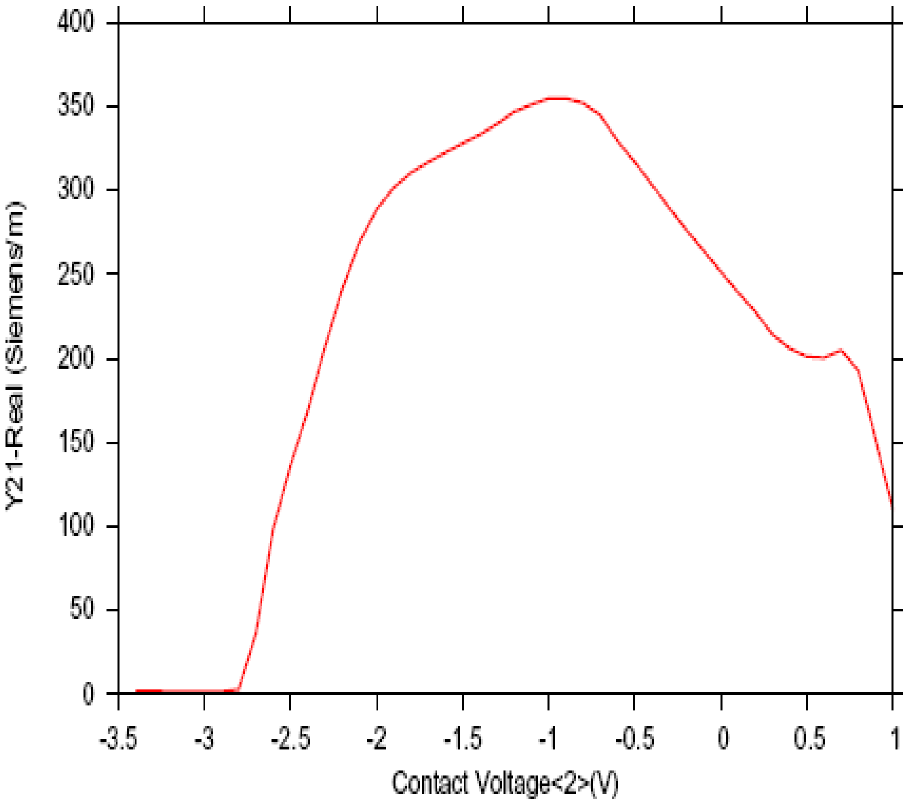
# Bell Shape In Gate Current

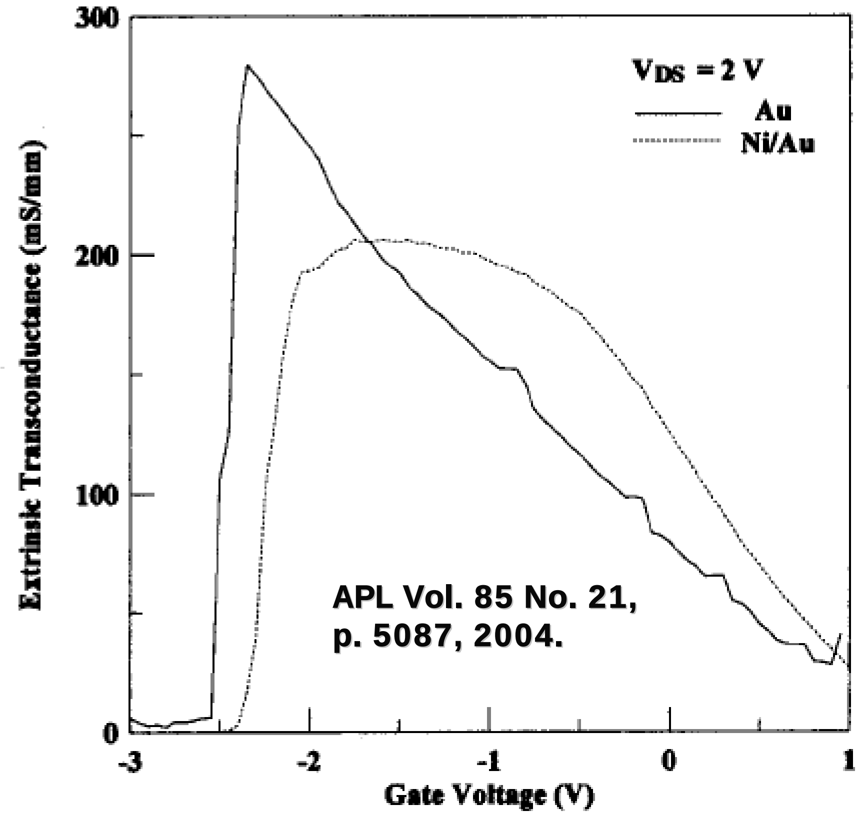



**Igs (upper left) vs Vgs & hole_Igs (lower left) vs Vgs curves (Vds at 2, 1.8, 1.6,1.4, 1.2 & 1 V upward). Notice the bell-shape with these curves. Due to difference in experimental structure, comparison of physical trend is intended here.**

# Simulated Transconductance




Simulated transconductance at Vds=2 V as compared with experiment on the right side. The quantitative difference may be due to uncertainty in contact resistances.

# Summary

- Impact ionization effect has been adequately accounted for by the APSYS software.
- Adjustment of contact and band structure may be used to optimize HEMT performance.
- Reasonable agreement with experimental measurement has been obtained.