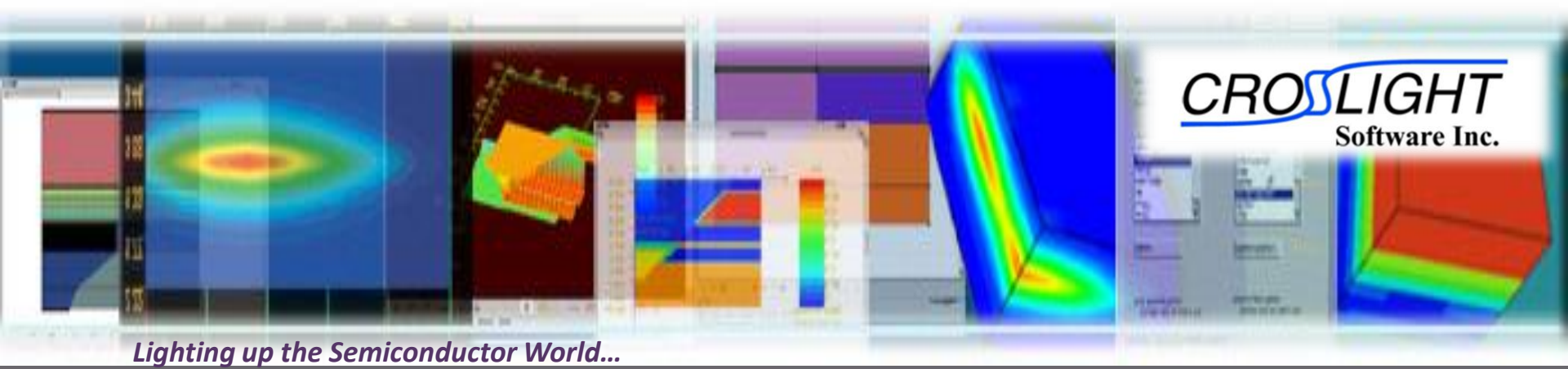


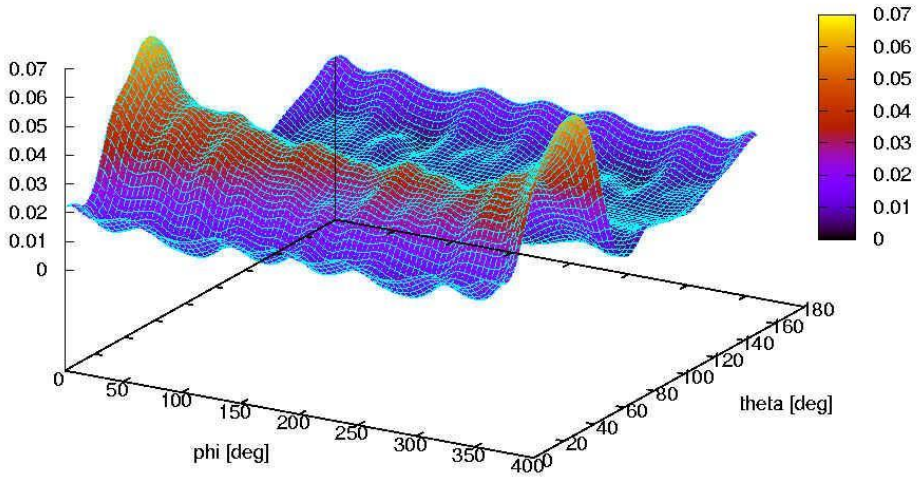
Lighting up the Semiconductor World…

3D Simulation of CMOS Image Sensor

www.crosslight.com

Outline

- Introduction to Crosslight TCAD
- About 3D TCAD Simulation and MaskEditor™
- Introduction to CMOS Image Sensor
- 3D Simulation of CMOS Image Sensor



A Glimpse

- A leading TCAD provider since 1993
- The world's No.1 TCAD simulator for optics and photonics application
- The world's first commercialized TCAD for Laser Diode
- Customer list extends to hundreds of companies, research institutions and universities world wide.
- Originally Crosslight is a spin-off of the National Research Council of Canada and later licensed the Suprem 4 from Stanford University to build CSuprem
- Complete product portfolio for 2D/3D semiconductor device simulation with great consistency between versions.
- *Café-time Simulator*. Windows based, user friendly GUI makes simulation more enjoyable.

Crosslight Global Offices

Vancouver Office

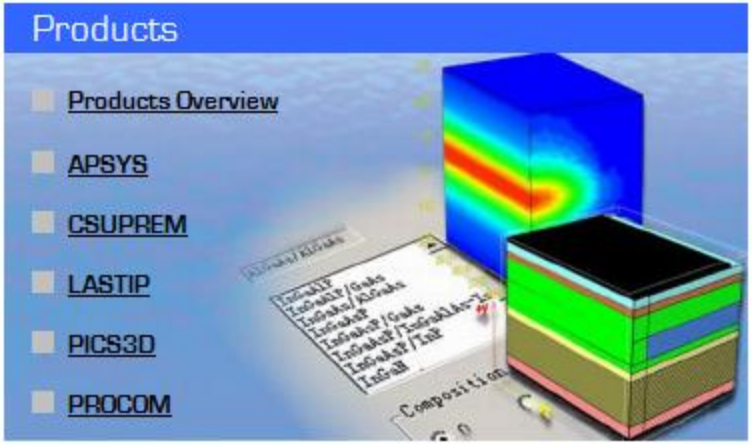
Japan Office

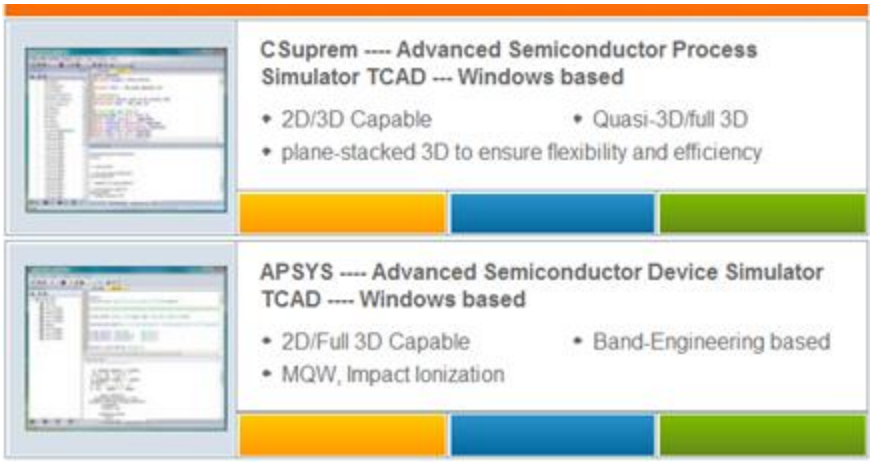
South Korea

China Office

- Vancouver Headquarter
  - Shanghai Office
    - Taiwan Distributor
    - China Distributor
    - India and Southeast Asia Distributor
  - Japan Office
    - Korea Distributor

Main Product Portfolio and Typical Applications

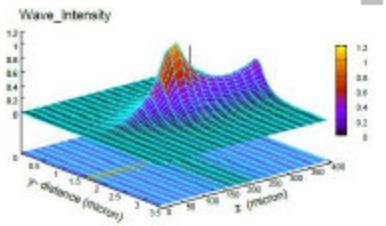




Optics and Photonics Applications

Solar Cells
- Solar Cell (Thin-film)
- Solar Cell (multi-junction)
- Solar Cell (crystalline/poly)

Photo Detectors
- Avalanche Photo Detectors
- CMOS Image Sensor
- QWIP



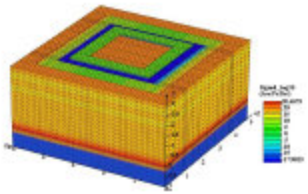
LEDs
- RC LED
- Organic LED (OLED)
- White OLED (WOLED)
- Quantum Dot LED
- Photonic Crystal LED
- Superluminescent LED
- MOCVD Growth

Laser Diodes
- Quantum Cascade Laser
- Edge Emitting Laser
- VCSEL
- Quantum Dot Laser

Microelectronics Applications

CMOS
- Nano-MOSFETs
- Strained Silicon
- CMOS Process

HEMT
- GaN HEMT
- GaAs HEMT
- MOCVD Growth



Power Devices
- BJT
- LDMOS
- Superjunction LDMOS
- Interconnect

MEMS (3D)

Advanced Physics

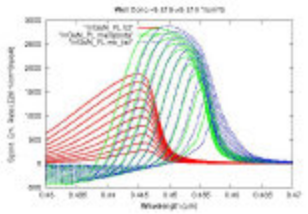
Advanced Device Physics

Quantum Drift and Diffusion

Intraband Quantum Tunneling Through Heterojunctions

Crystal orientation on Optical property of GaN Devices

Manybody, Exciton and inhomogeneous Broadening Effects



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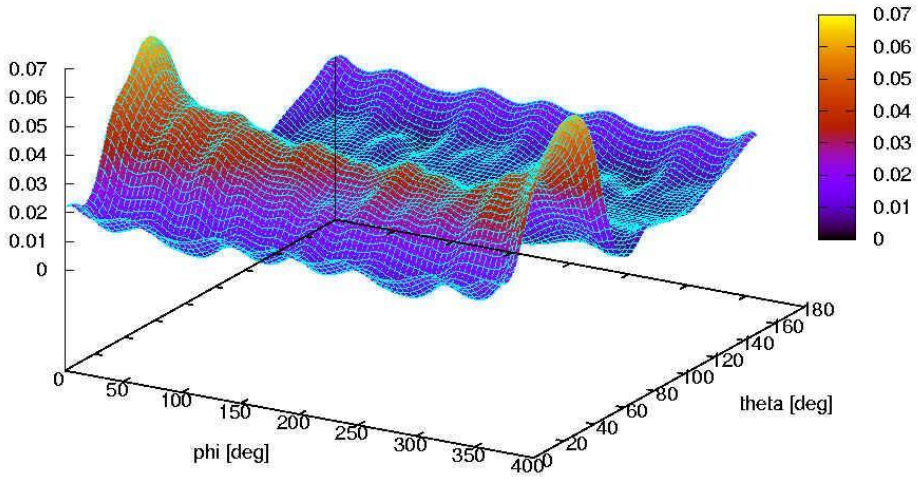


About3D Simulation

Why 3D?

- Device is 3D in nature, lot's of devices need 3D simulation for better accuracy. For example, CMOS Image Sensor, Superjunction LDMOS, metal interconnect, etc.

Do you need 3D Simulation?

- Does your device have third (z) dimension variations?
- Do you want to exam some peripheral behavior of the device, like fringe current at the corner of race-track shaped gate?
- Does your device have a special shape from top down view? (like CMOS Image Sensor, or HEXFET)?

Challenges for 3D Simulation:

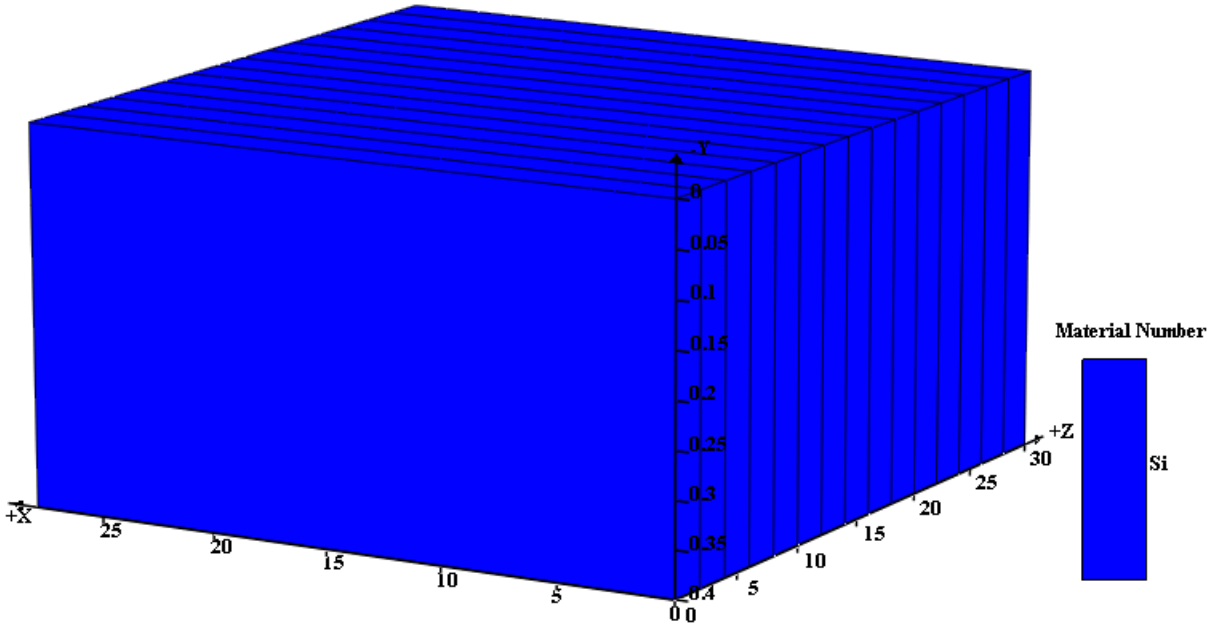
- Extremely time consuming. Believe or not, traditional 3d simulation time may be longer than real process time for large power semiconductor devices.
- Difficult to build the structure and optimize the mesh.

Crosslight's Approach of 3D Simulation

Stacked3D

- Crosslight has developed a unique 3D simulation package. Instead of traditional approach, which basically starts from bulk (conventional 3D FEM), Crosslight starts from 2D planes, and stack them to form the 3D structure.

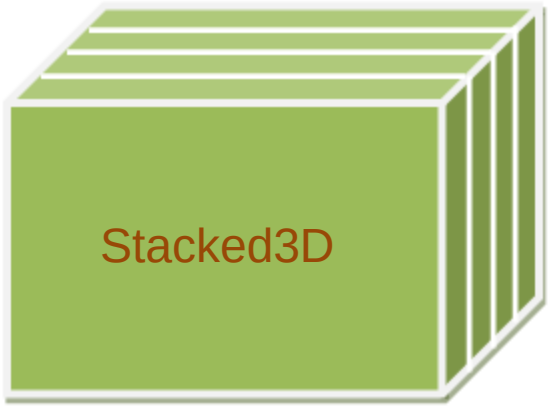
Stacked3D Example:

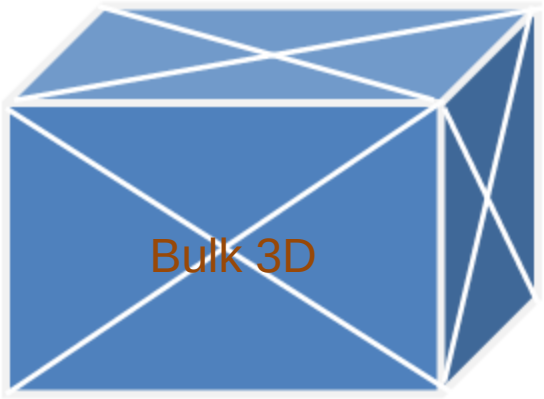


Advantages of Stacked3D

Stacked3D Advantages

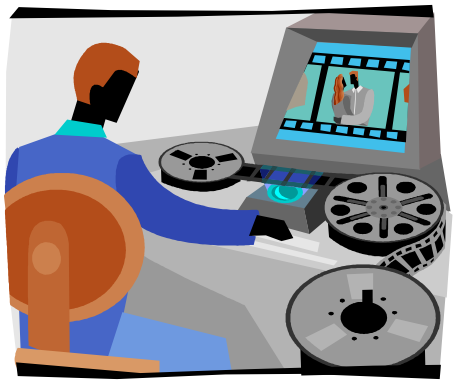
- Highly Efficient, generally less mesh points required, mesh density can easily be varied
- Easy to build: It starts from 2D planes
- Easy to optimize mesh. The mesh can be optimized for individual planes
- Increased 3D success rate from successful 2D simulation
- Directly extract 2D planes and 2D simulation





Introducing the New MaskEditor™ and SemiCrafter™

What's MaskEditor/SemiCrafter?



- A powerful 3D mask editing tool for 3D simulation

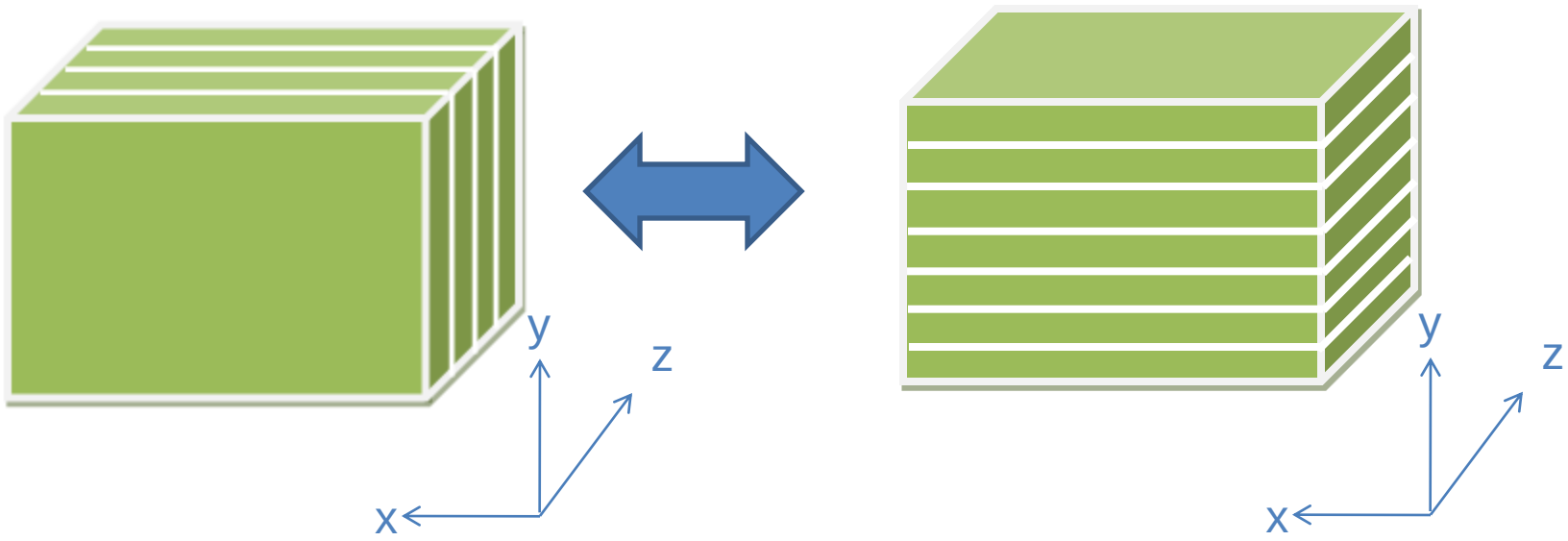
What are the Applications?

- MaskEditor is a general purpose layout tool
- Works seamlessly with CSuprem to create 3D structure for virtually all types of semiconductor devices, like MOSFET, BJT, LED, etc.

What are the Basic Functions of MaskEditor/SemiCrafter?

- Creates device layout files in GDSII format from scratch (Beta).
- Auto cutting and generate masks needed for 3D Csuprem process simulation.

The Difference between MaskEditor™ and SemiCrafter™

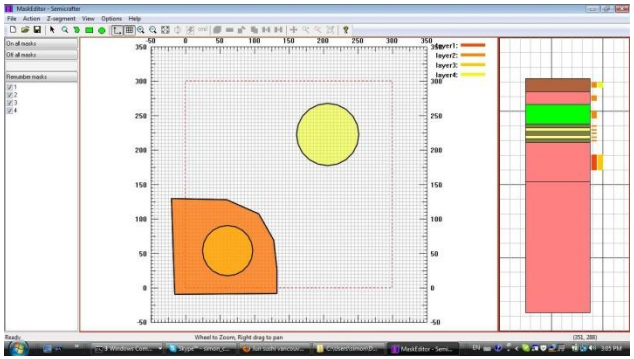


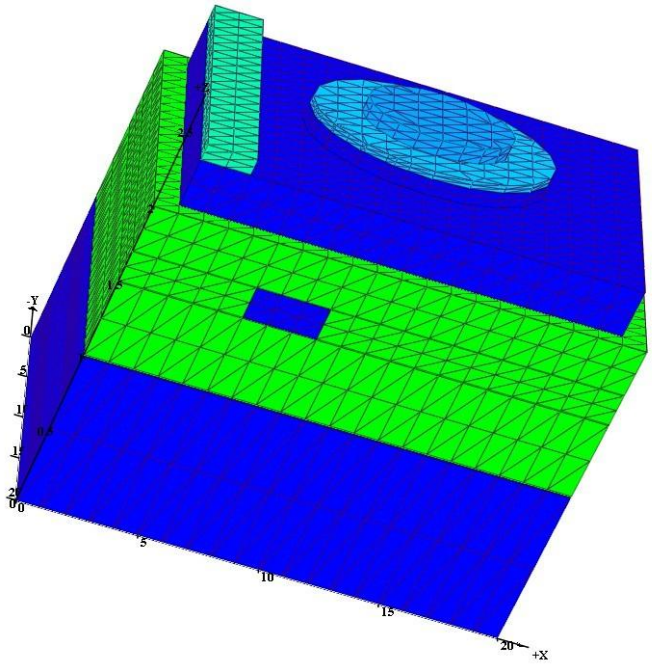
MaskEditor™

SemiCrafter ™

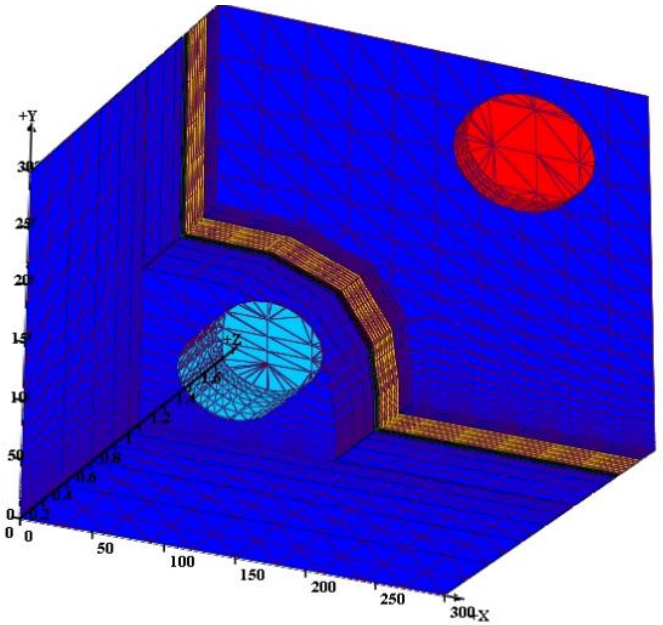
Examples of SemiCrafter™

LED and Micro Disk Laser Diode Examples

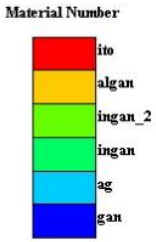




Micro Disk Laser Diode



LED



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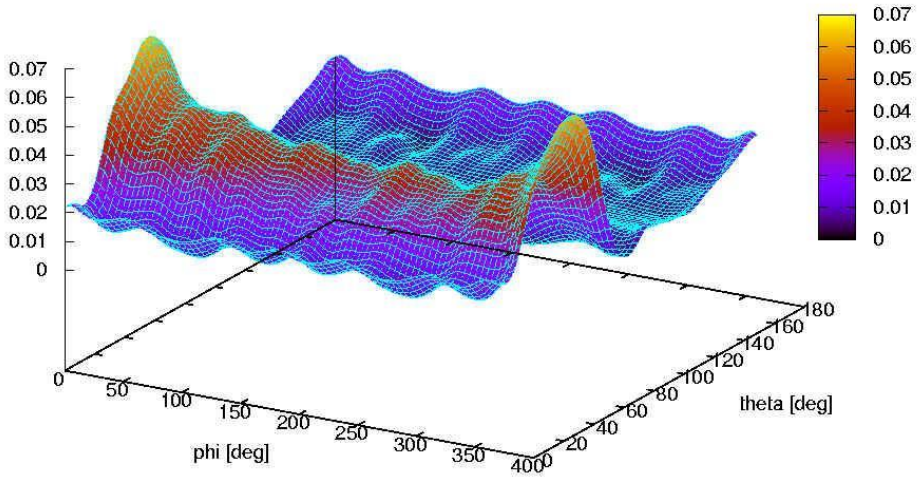
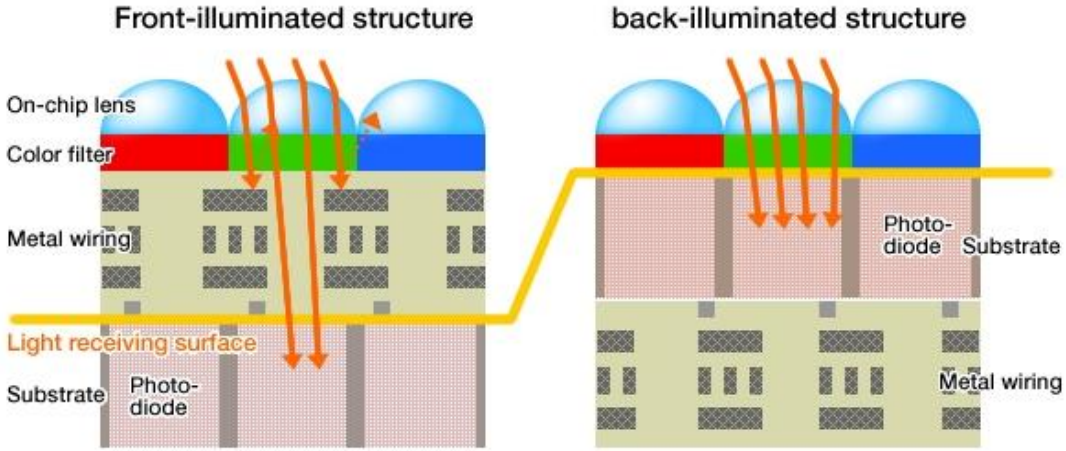
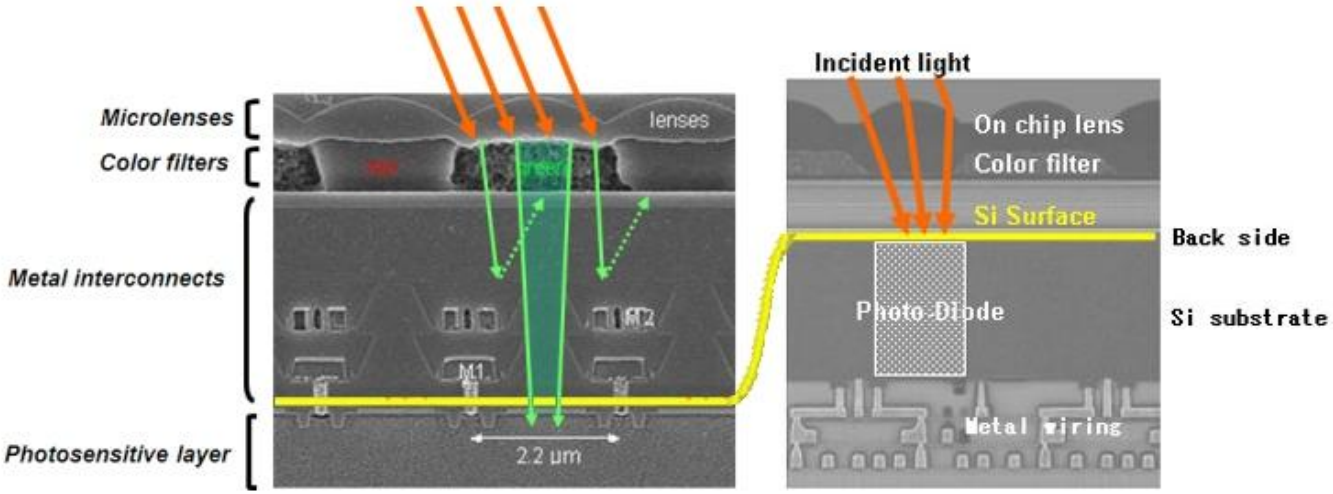


The Application of CMOS Image Sensor

Introduction To CMOS Image Sensor

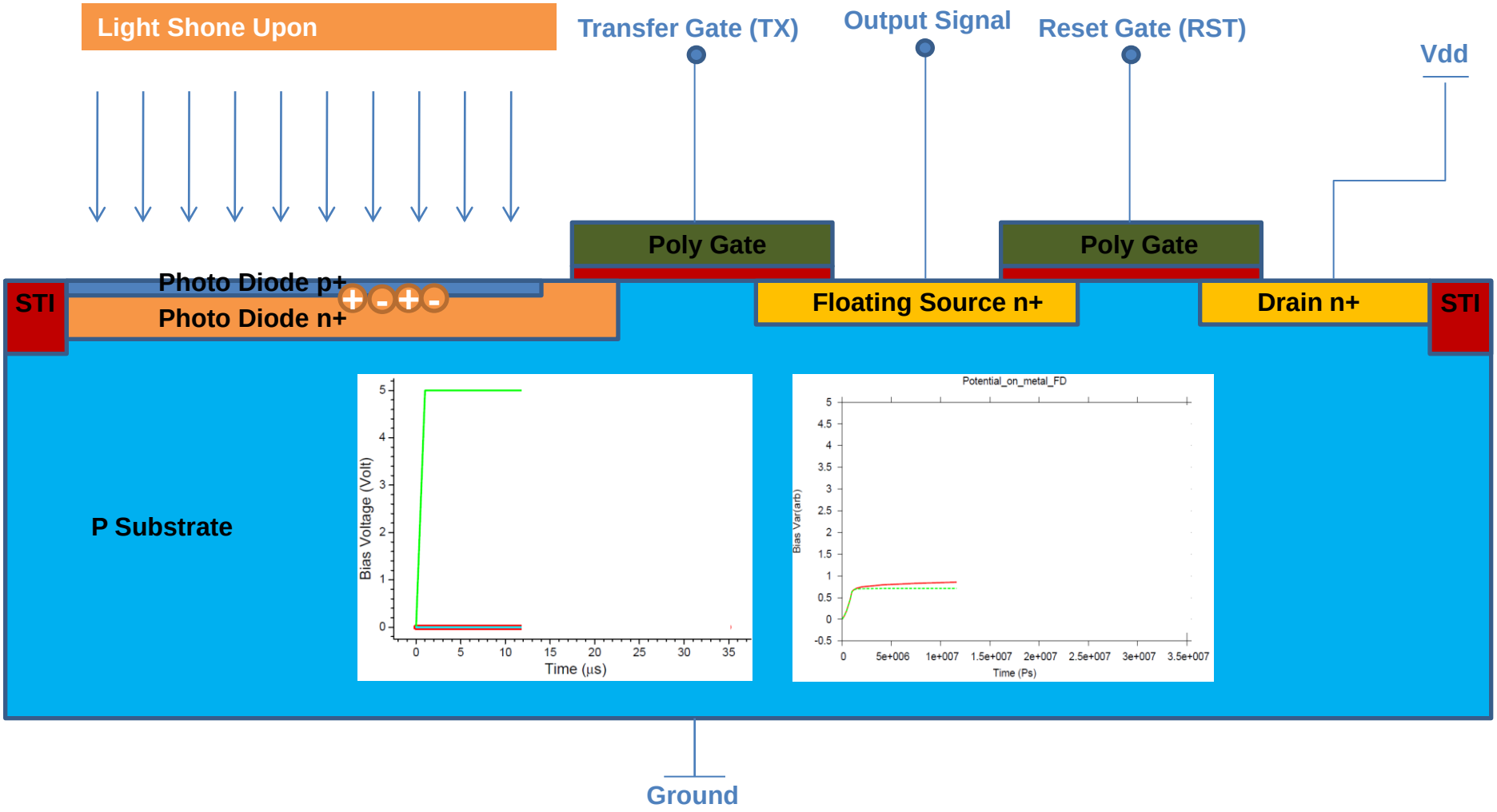
Canon CMOS Image Sensor



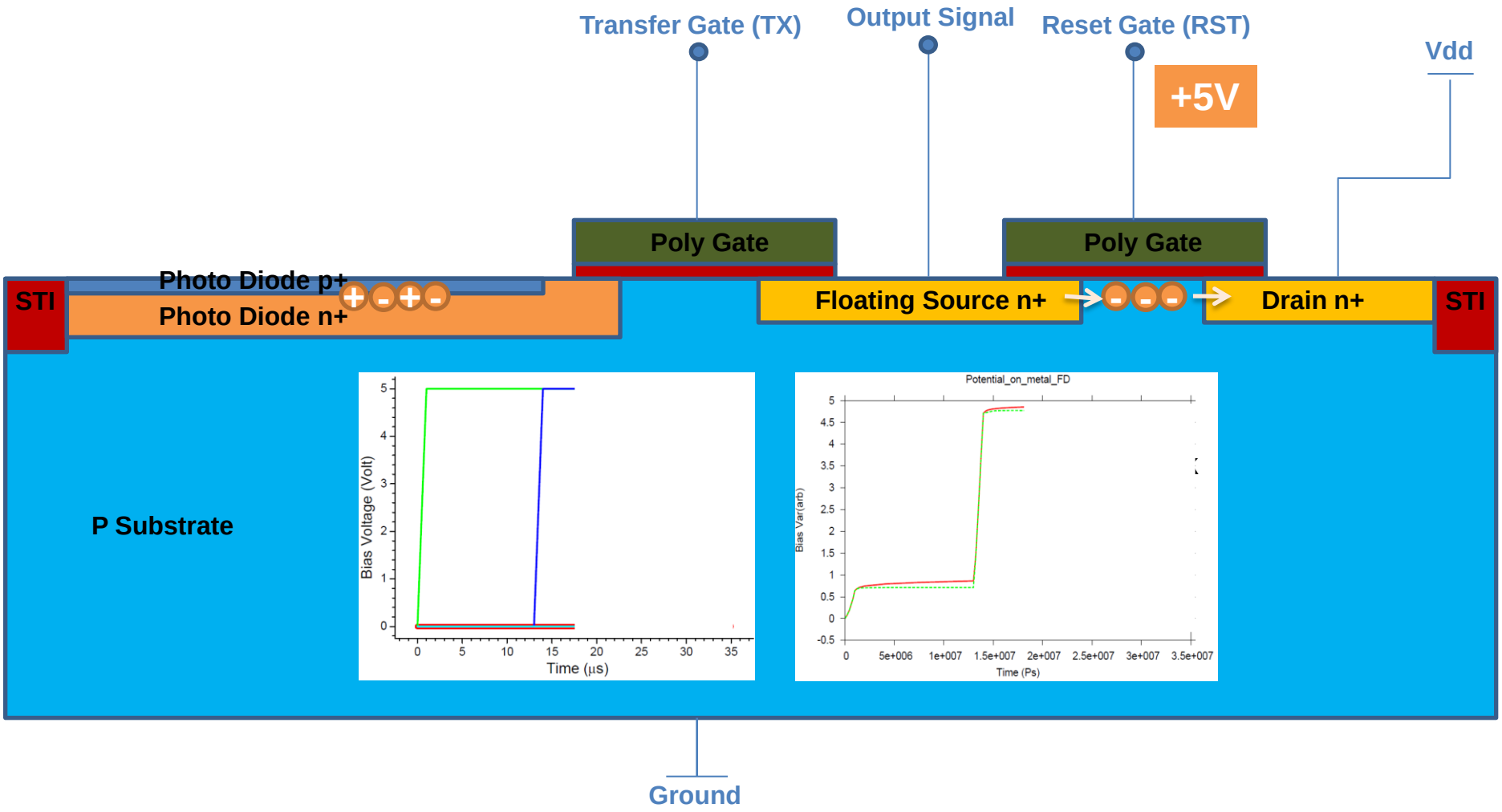


Source: http://www.i-micronews.com/lectureArticle.asp?id=1607
http://www.usa.canon.com/dlc/controller?act=GetArticleAct&articleID=246

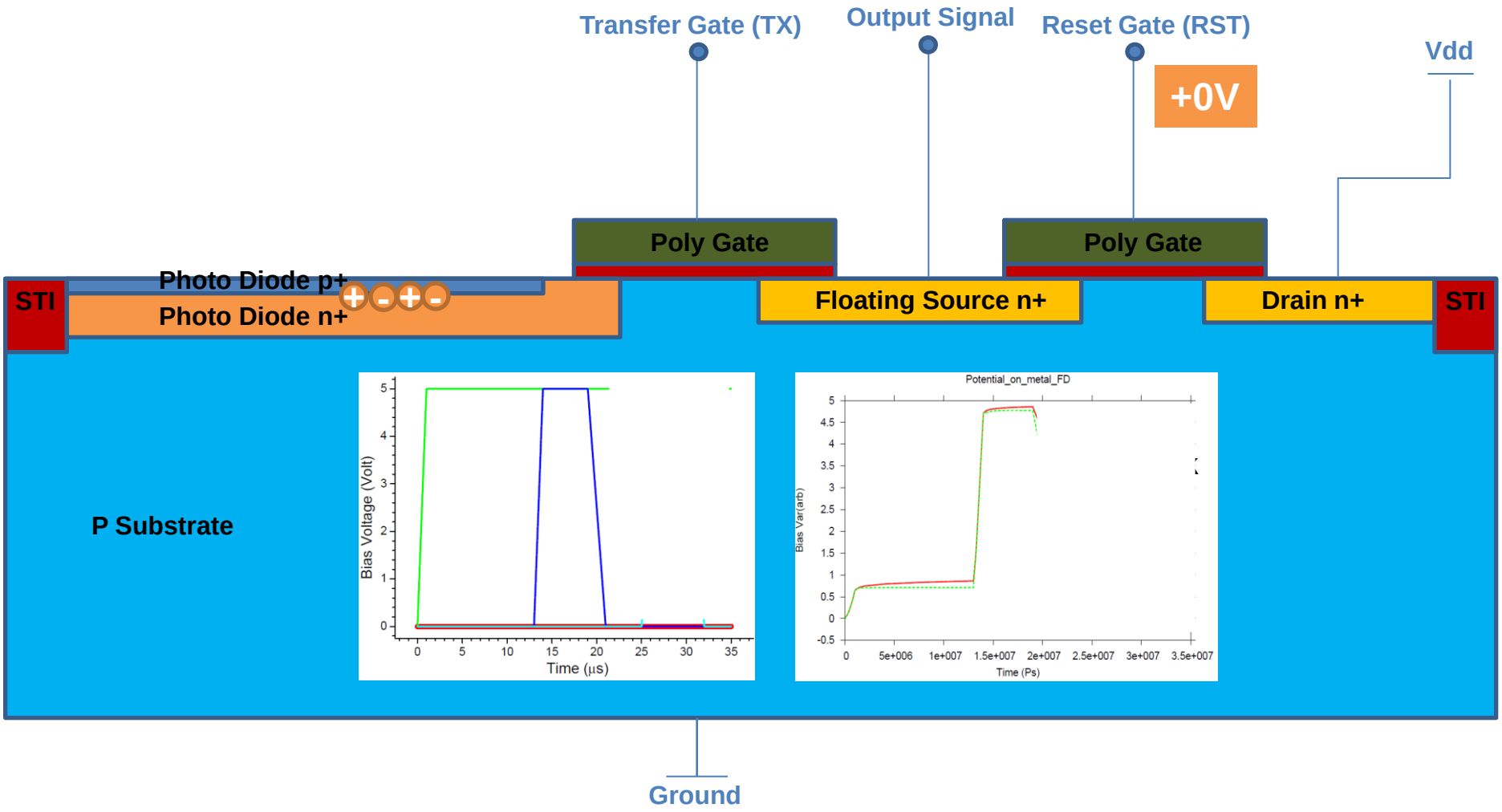
Simplified Simulation Structure and Bias



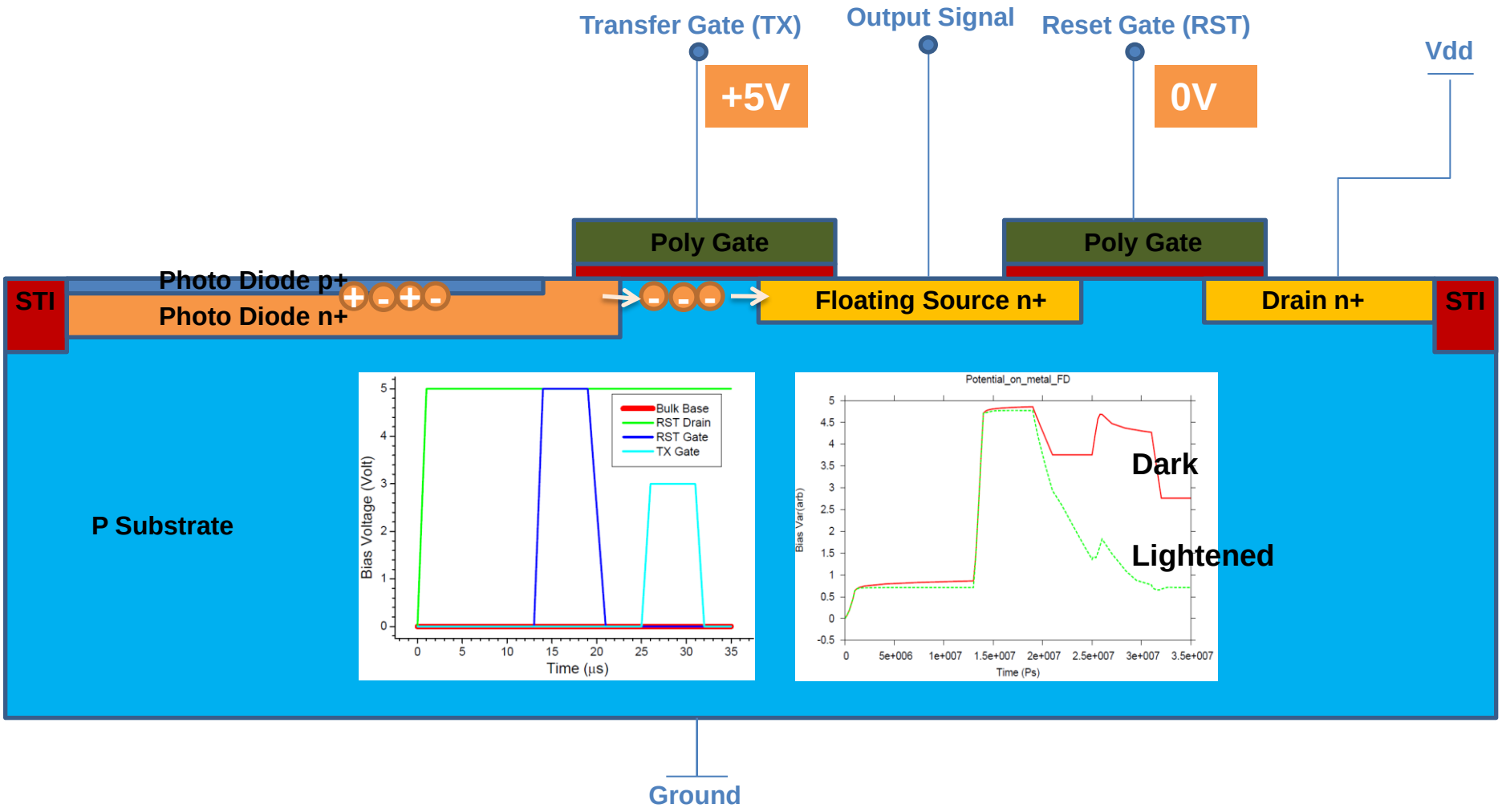
Reset Gate (RST) Turned On



Reset Gate (RST) Turned Off



Transfer Gate (TX) Turned On



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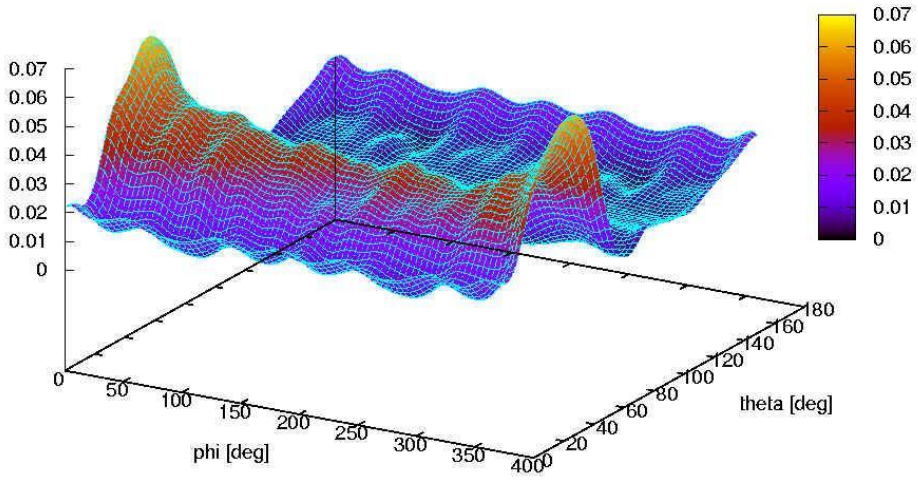
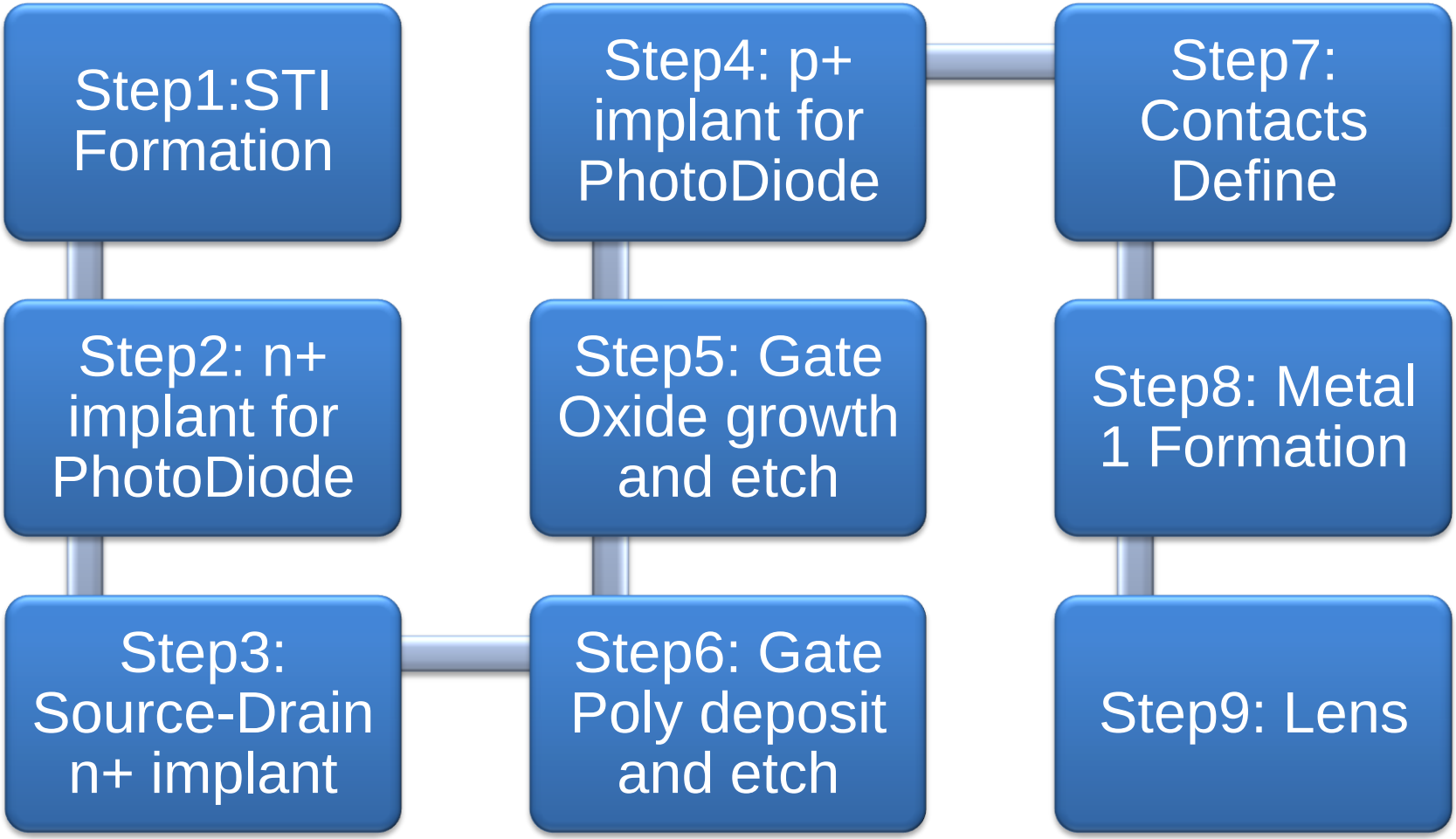
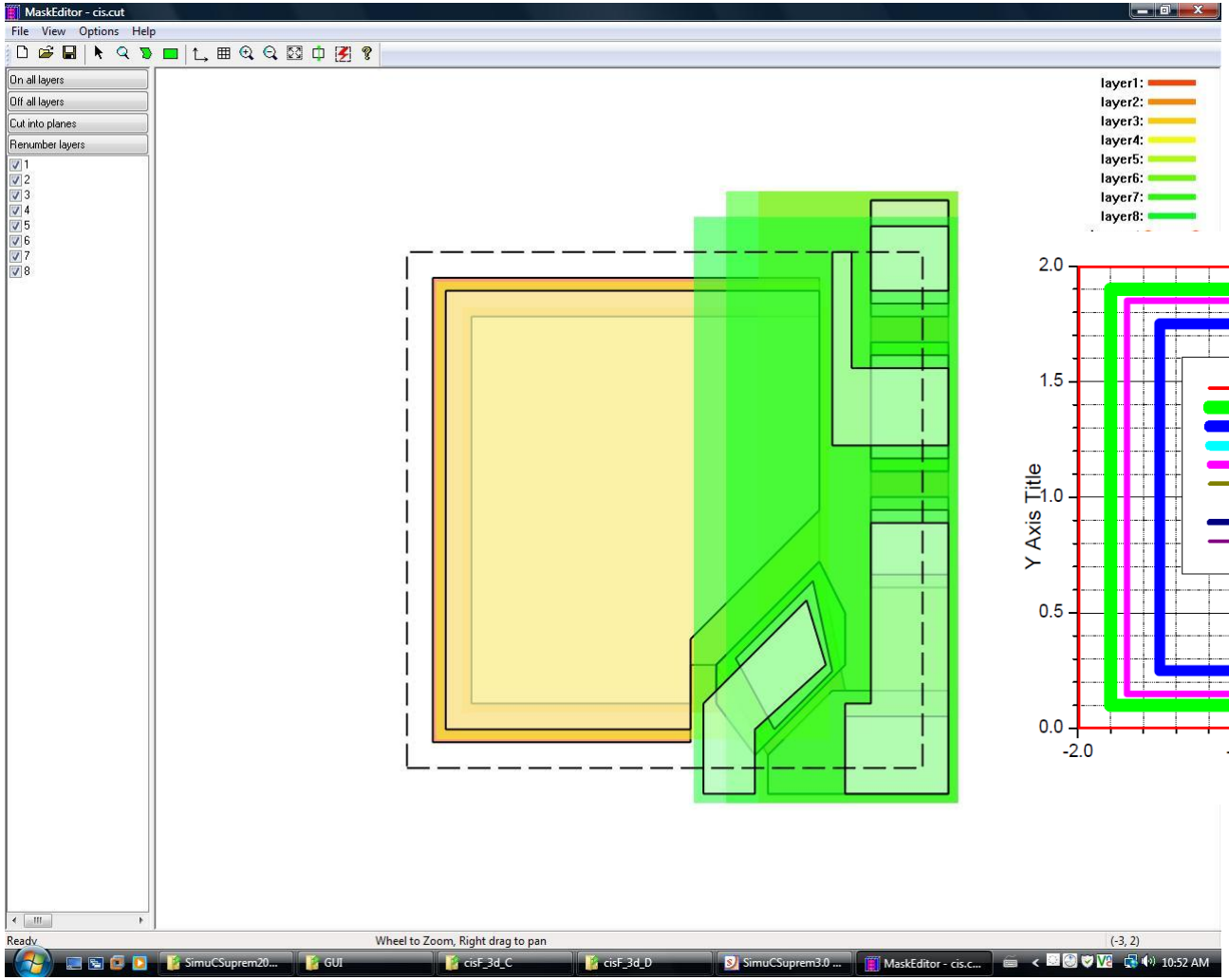
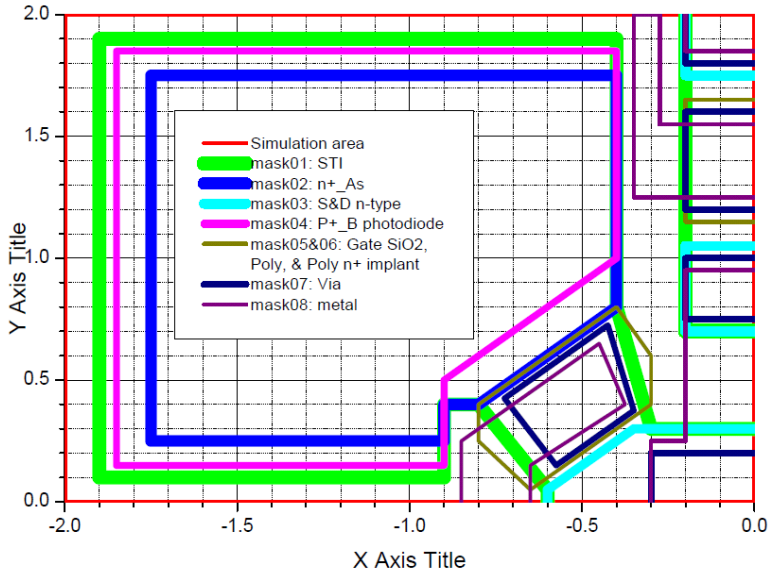


Overview of Fake CMOS Image Sensor Process

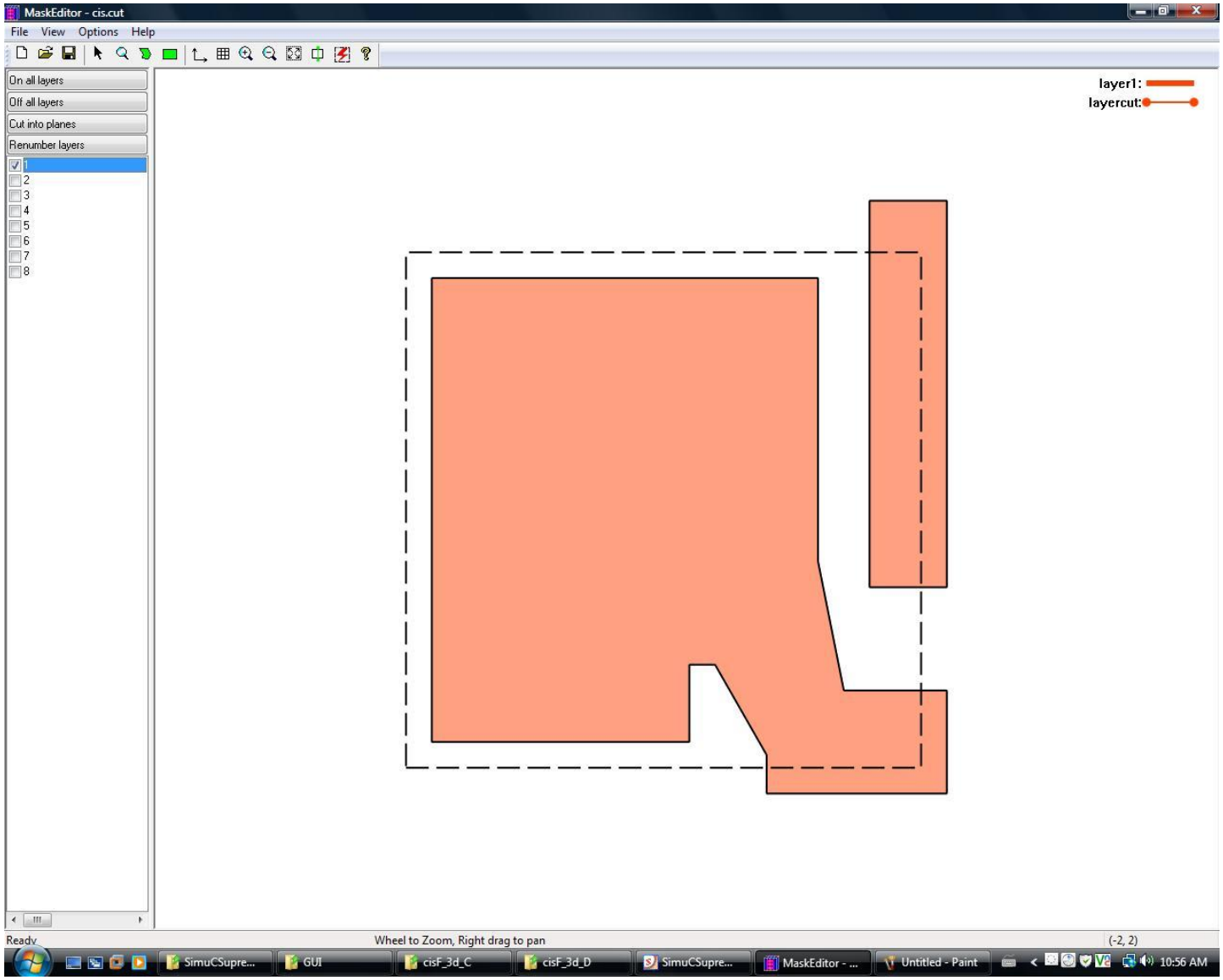


Mask Sets

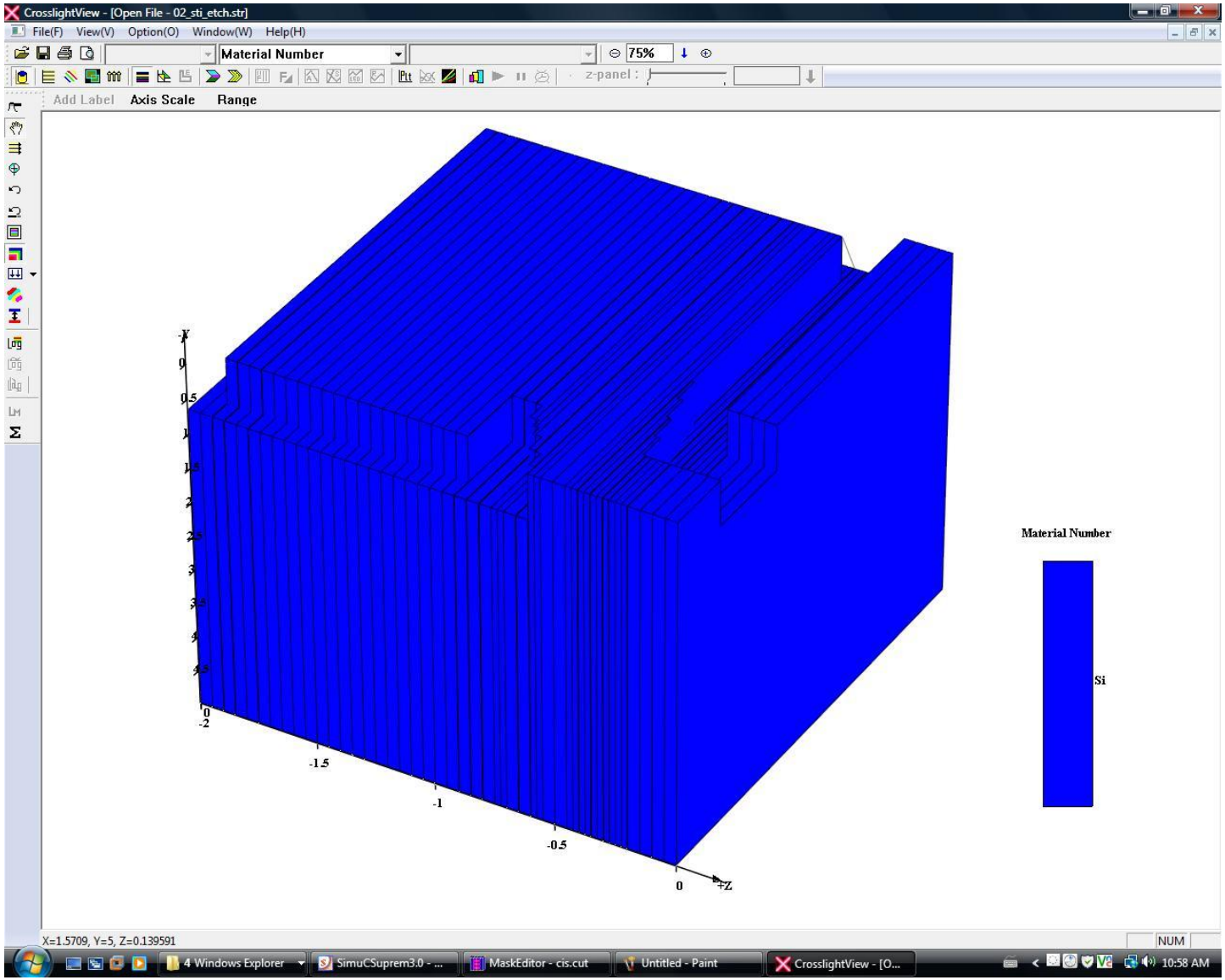

MaskEditor - cis.cut
File View Options Help
On all layers
Off all layers
Cut into planes
Renumber layers
1
2
3
4
5
6
7
8
layer1:
layer2:
layer3:
layer4:
layer5:
layer6:
layer7:
layer8:
Ready
Wheel to Zoom, Right drag to pan
(-3, 2)
10:52 AM


Simulation area
mask01: STI
mask02: n+_As
mask03: S&D n-type
mask04: P+_B photodiode
mask05&06: Gate SiO2, Poly, & Poly n+ implant
mask07: Via
mask08: metal
Y Axis Title
X Axis Title
2.0
1.5
1.0
0.5
0.0
-2.0
-1.5
-1.0
-0.5
0.0

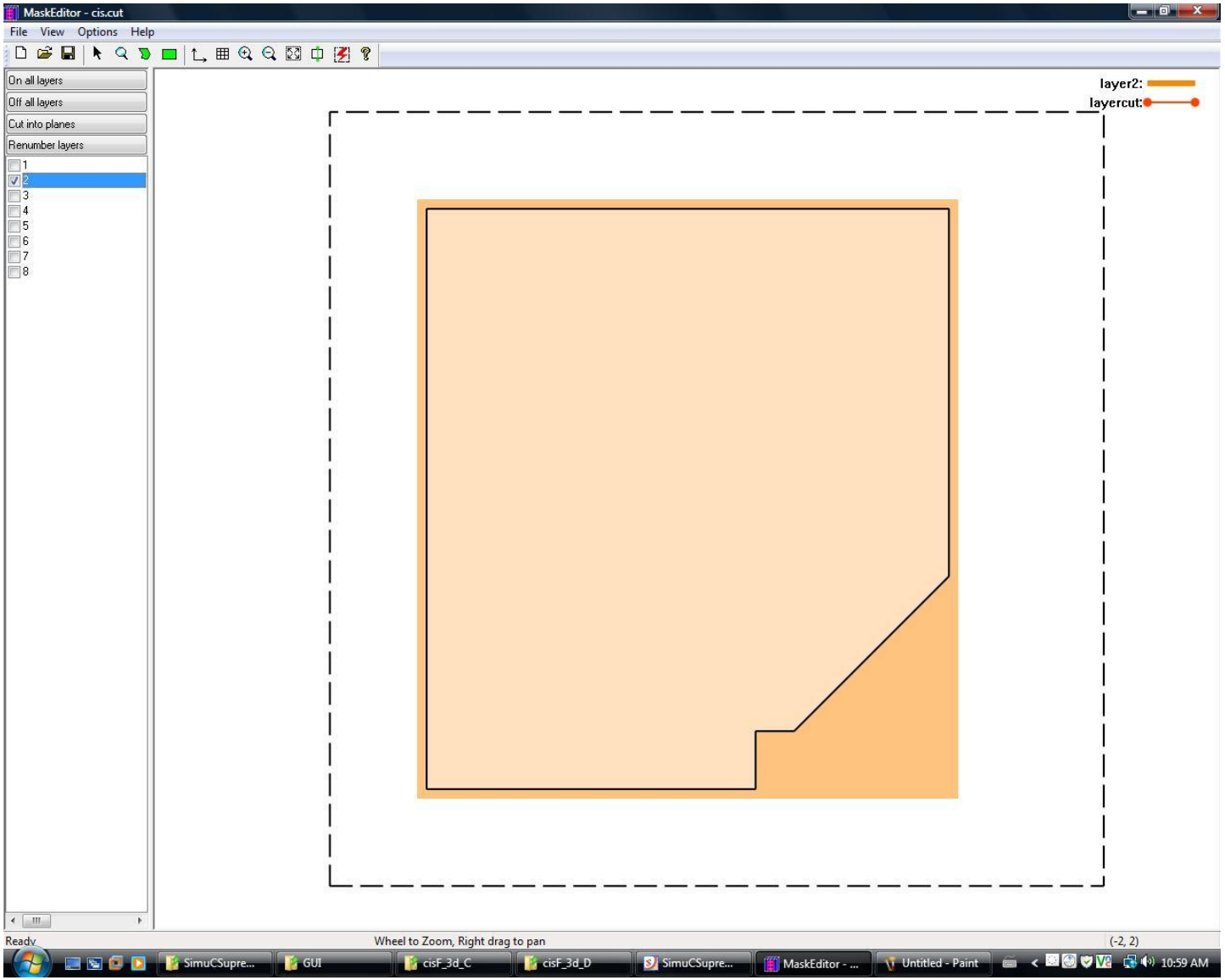
Mask Set 01 – STI



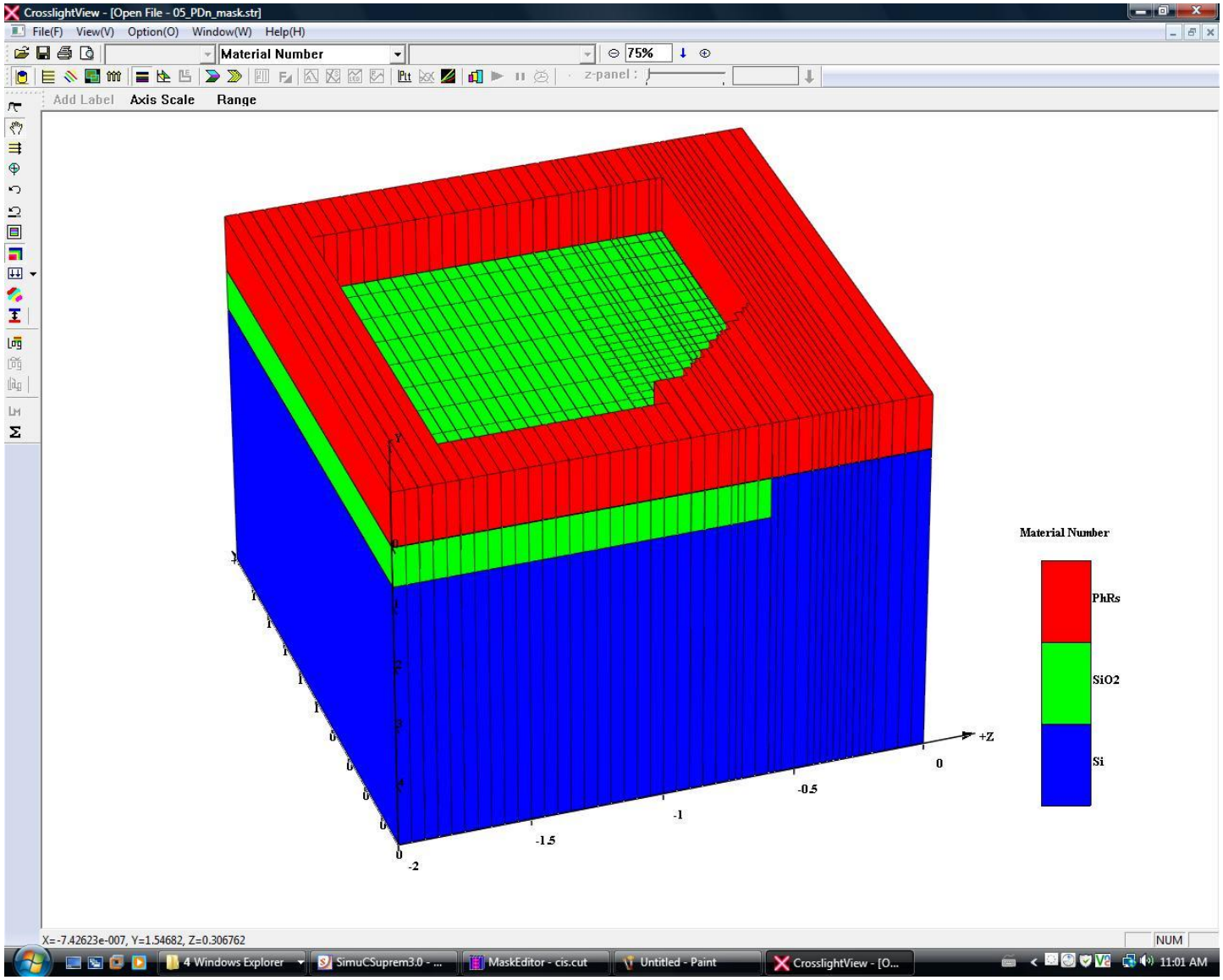
Silicon Etch for STI (Mask Set 01)



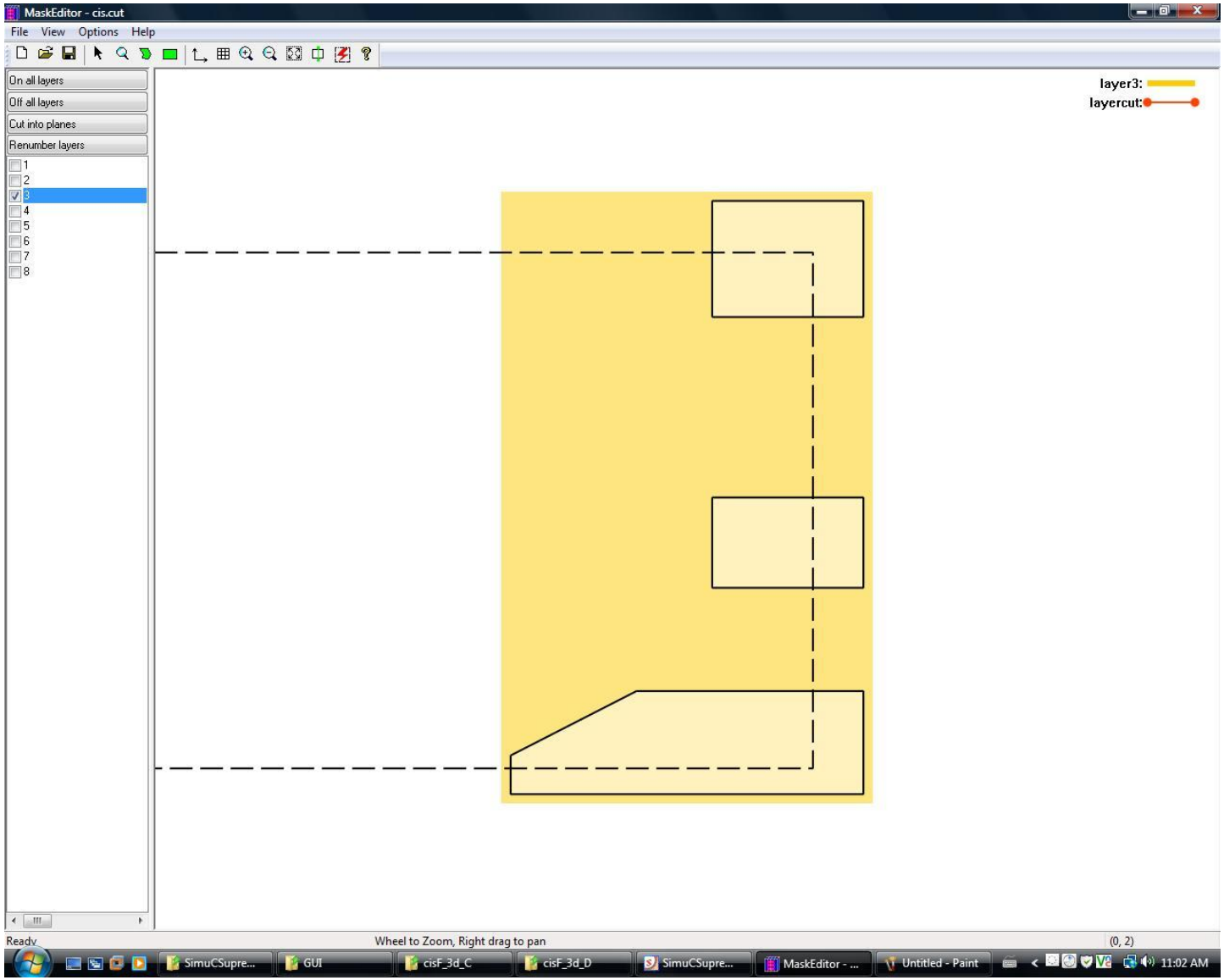
Mask Set 02 – n^+-Implantation for PD



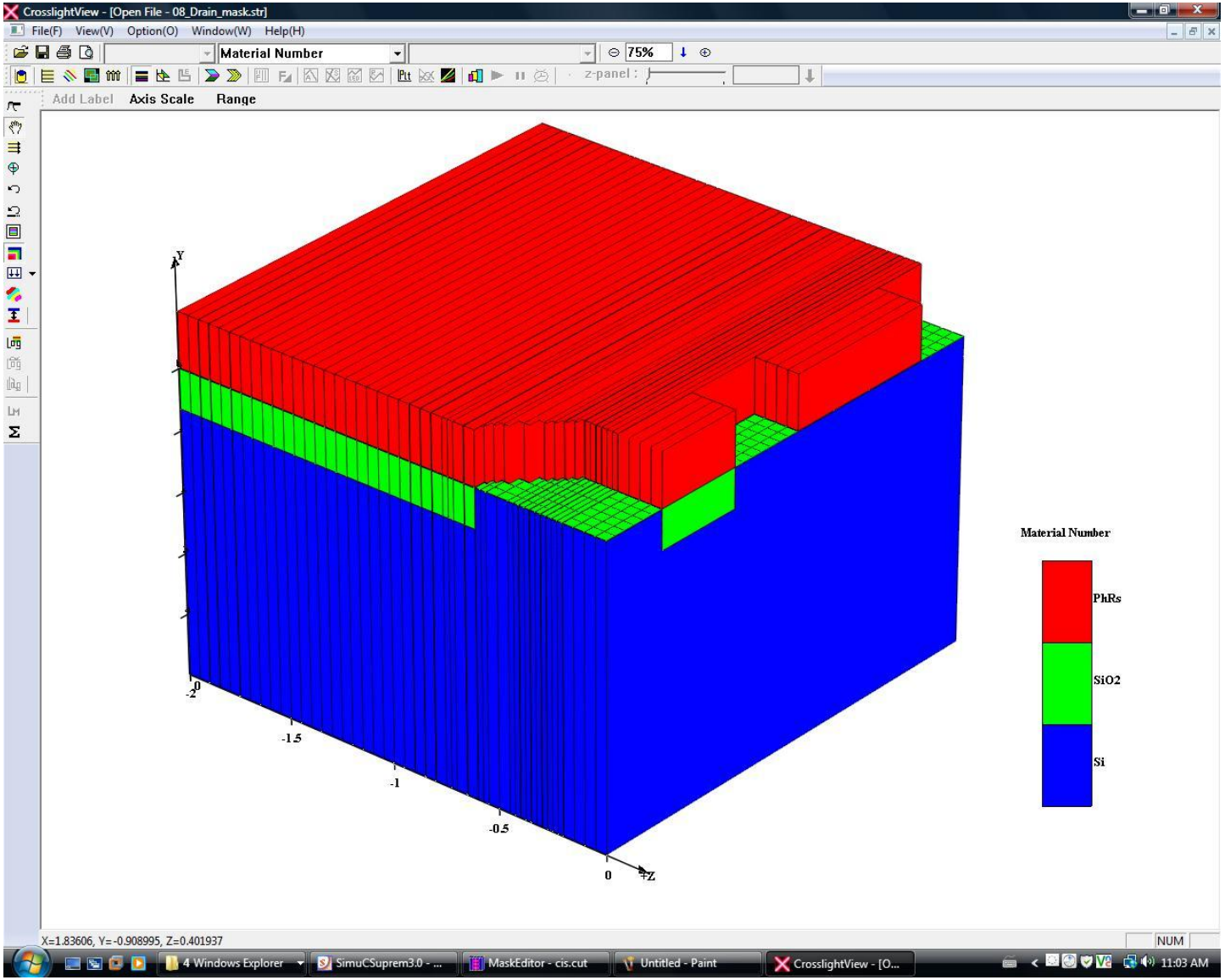
Photoresist for Mask Set 02



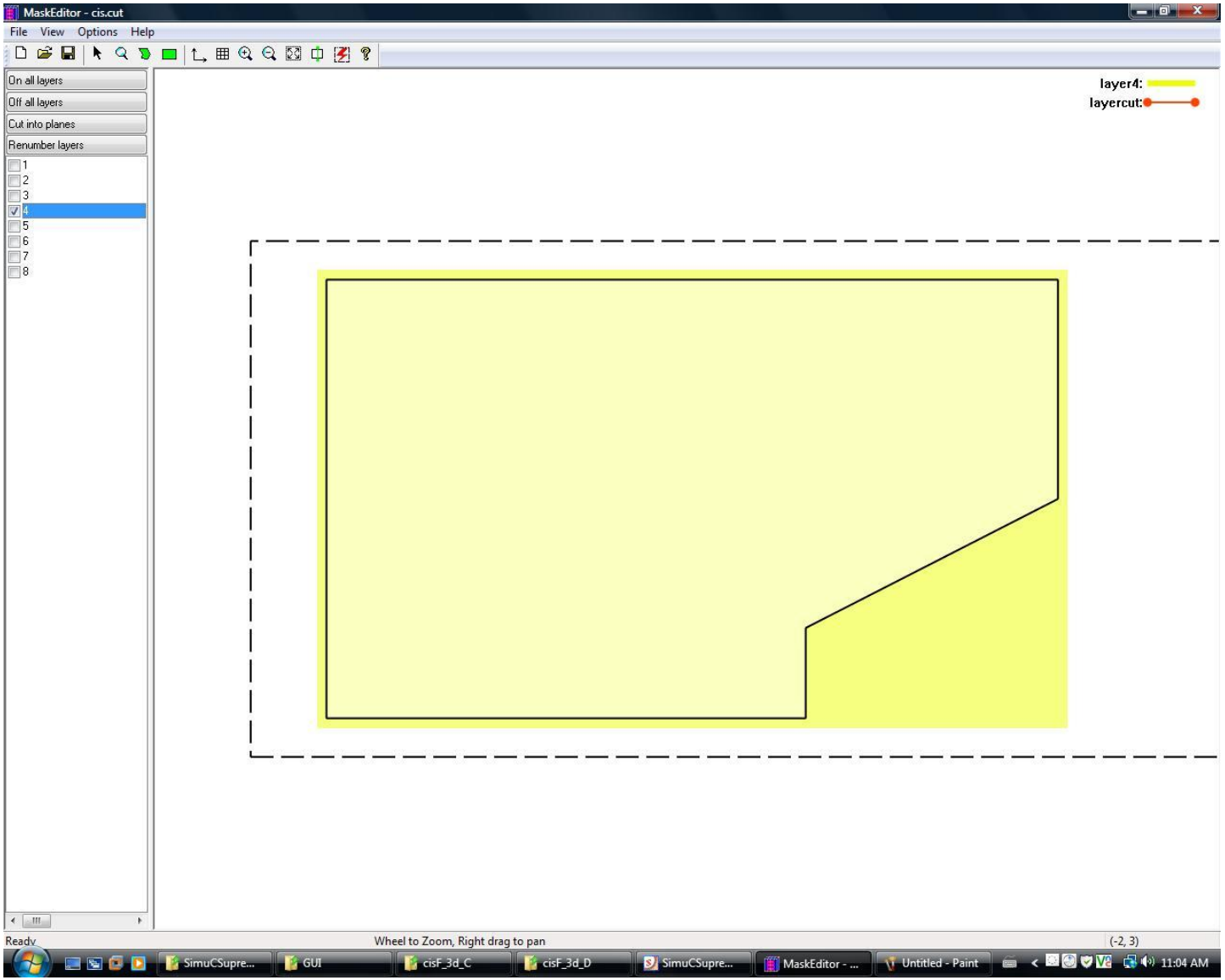
Mask Set 03 – S & D n-Implantation



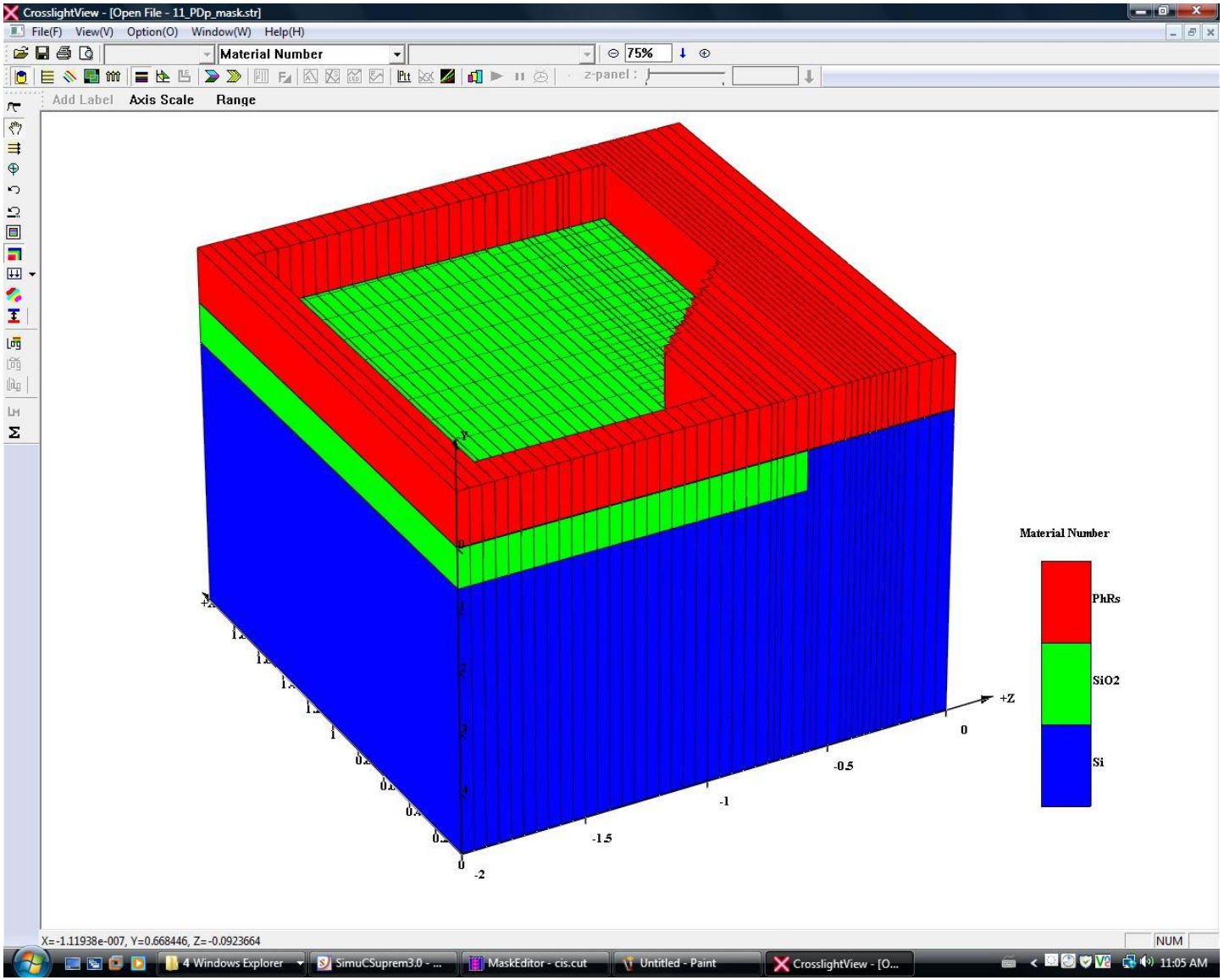
Photoresist for Mask Set 03



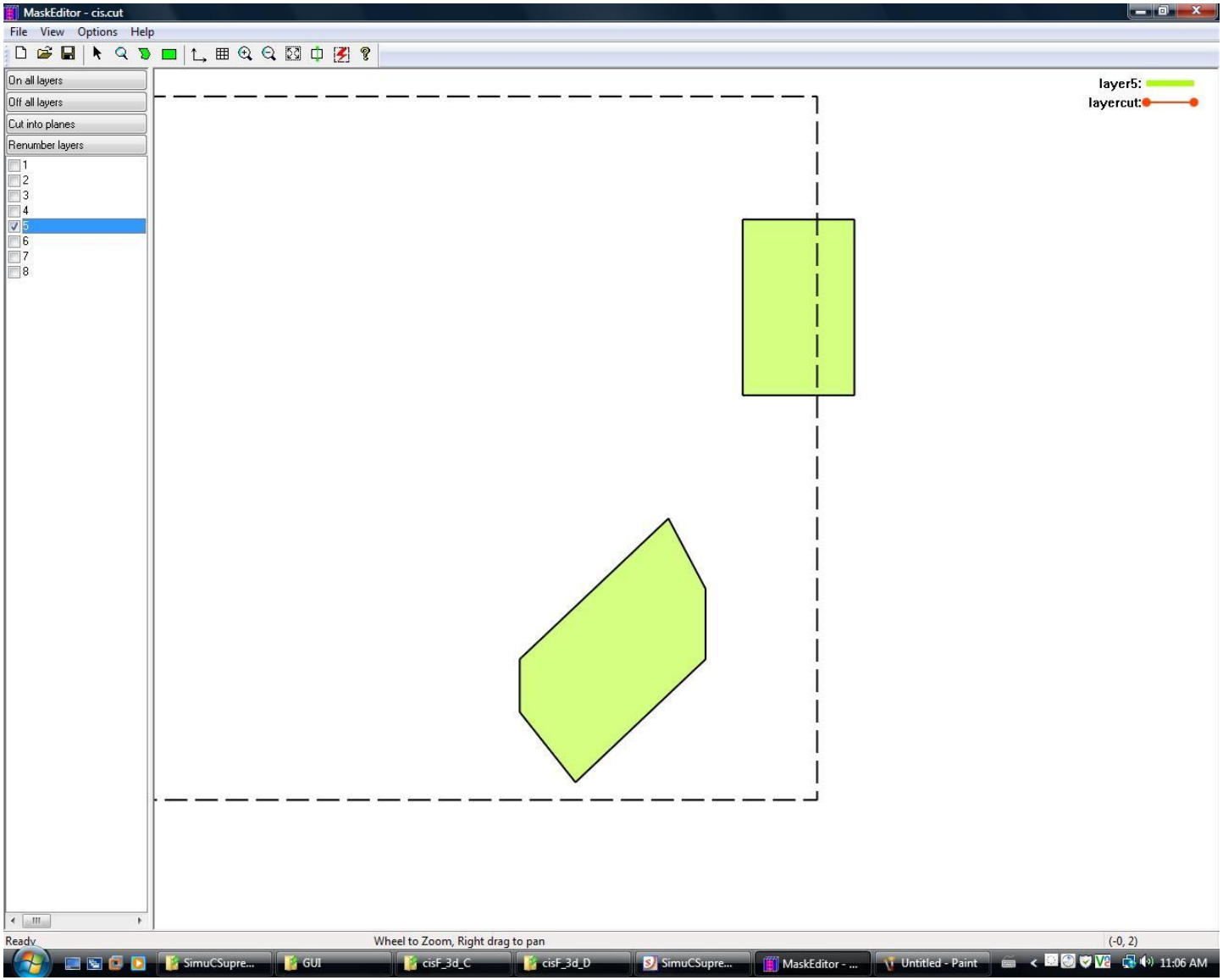
Mask Set 04 – p^+-Implantation for PD



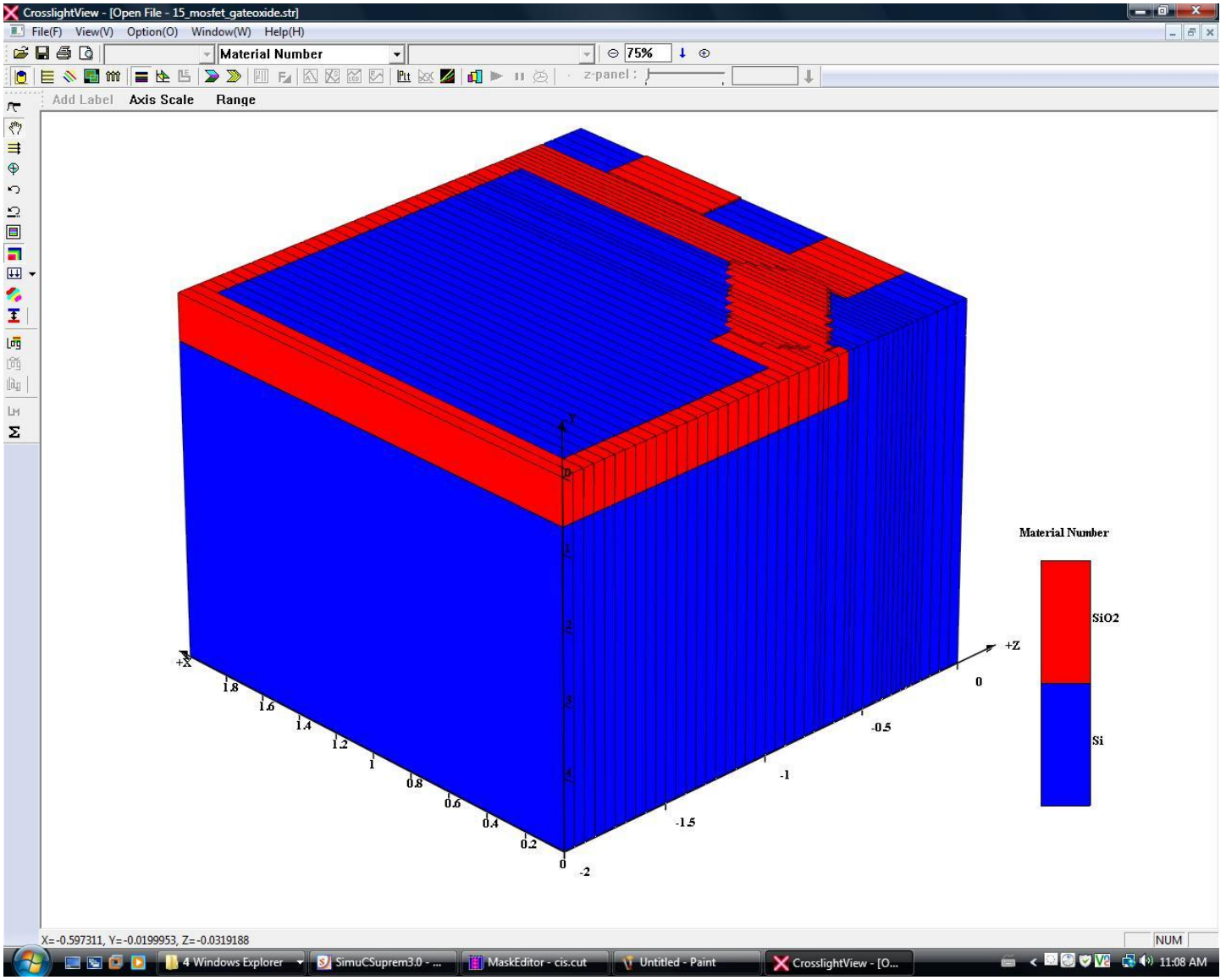
Photoresist for Mask Set 04



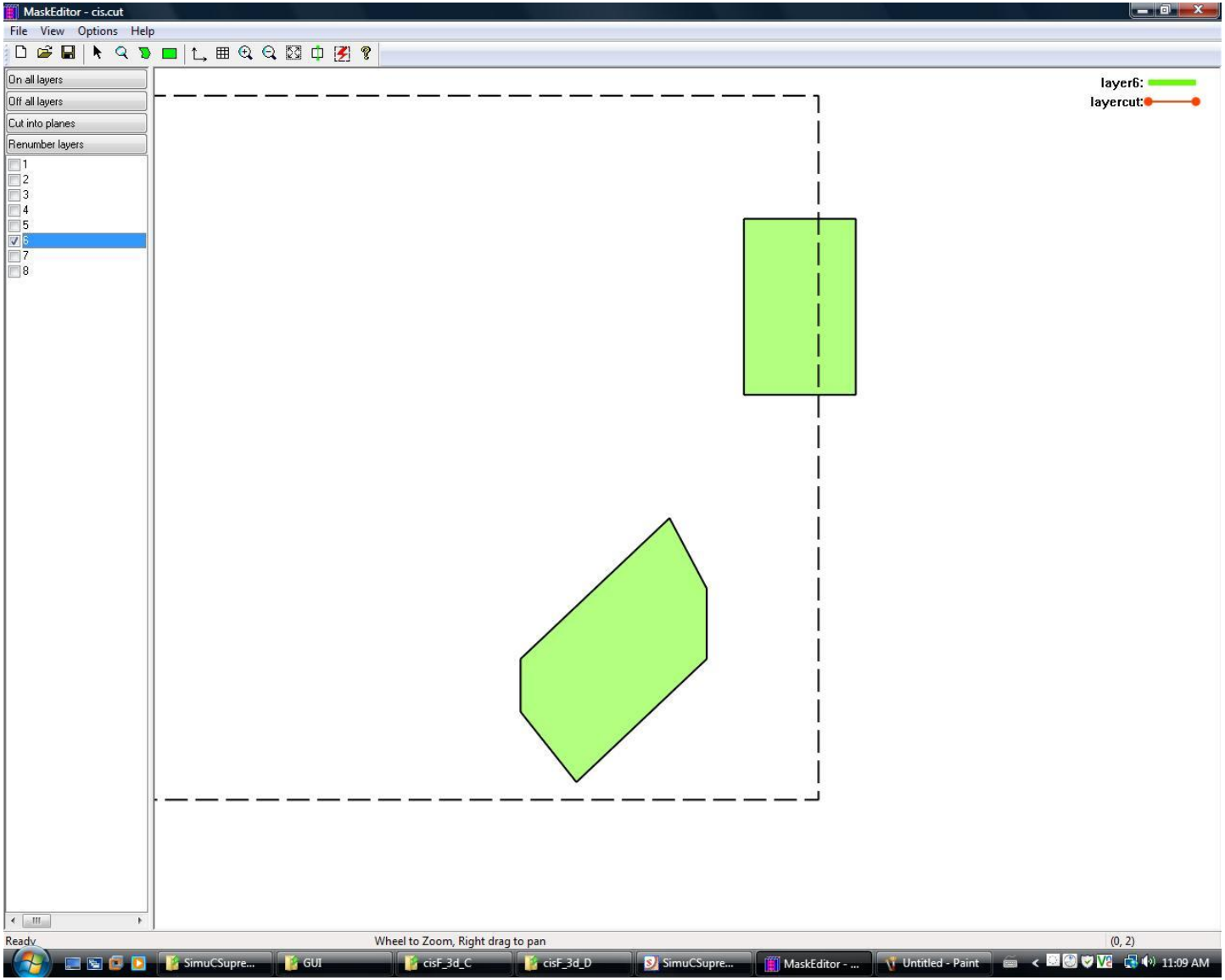
Mask Set 05 – Gate Oxide



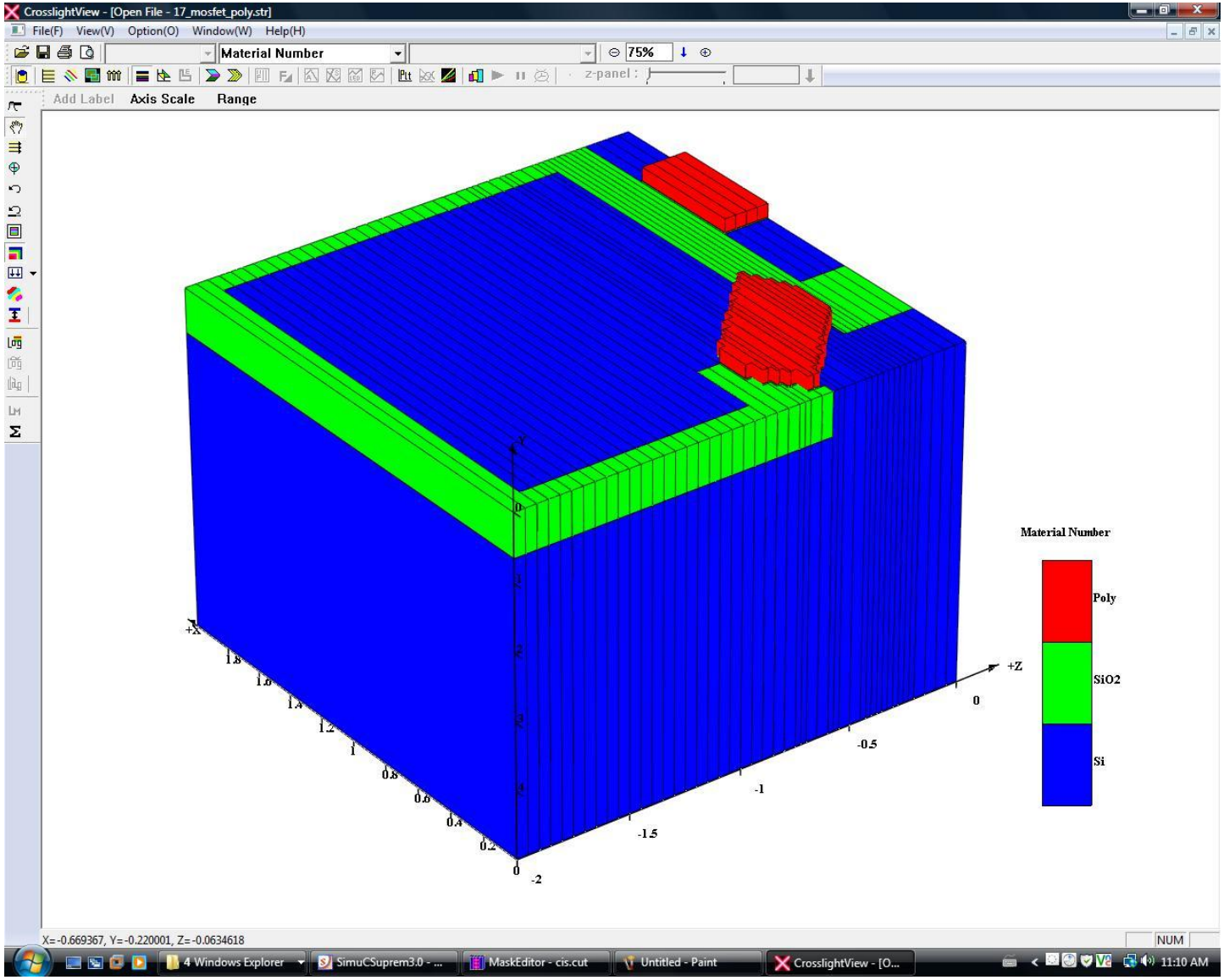
Oxide After Etch (Mask Set 05)



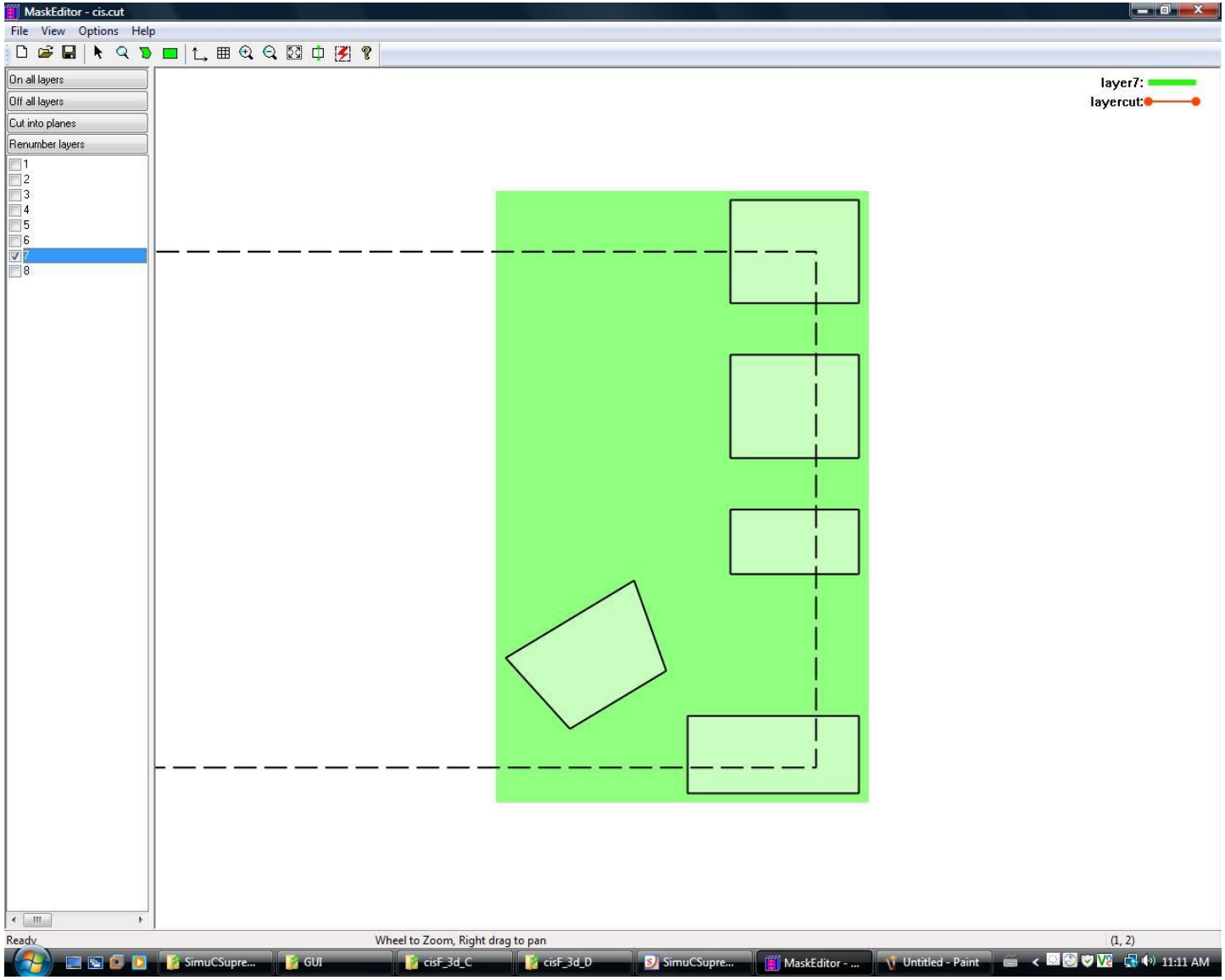
Mask Set 06 – Gate Poly Si



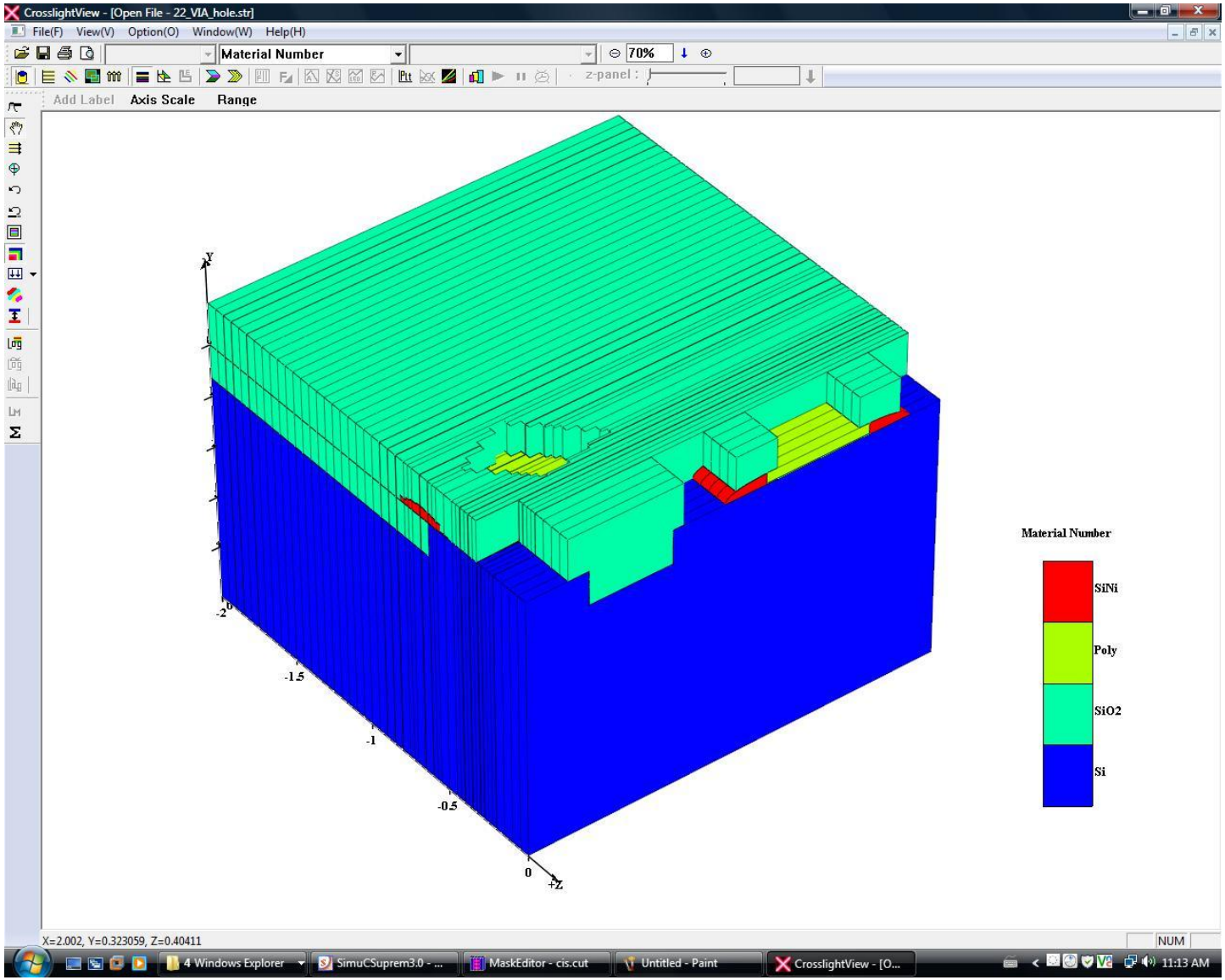
Gate Poly Etch (Mask Set 06)



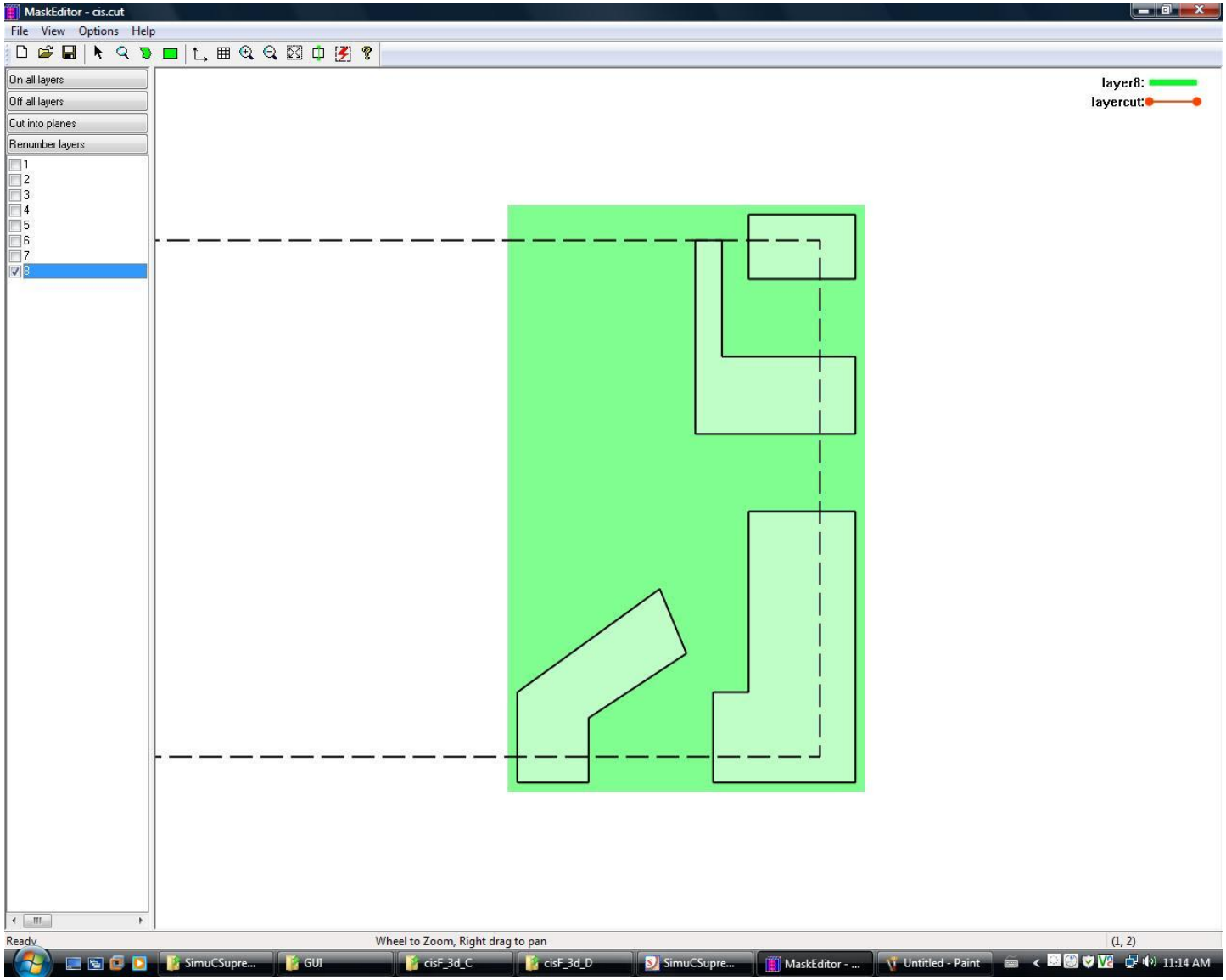
Mask Set 07 – Contacts



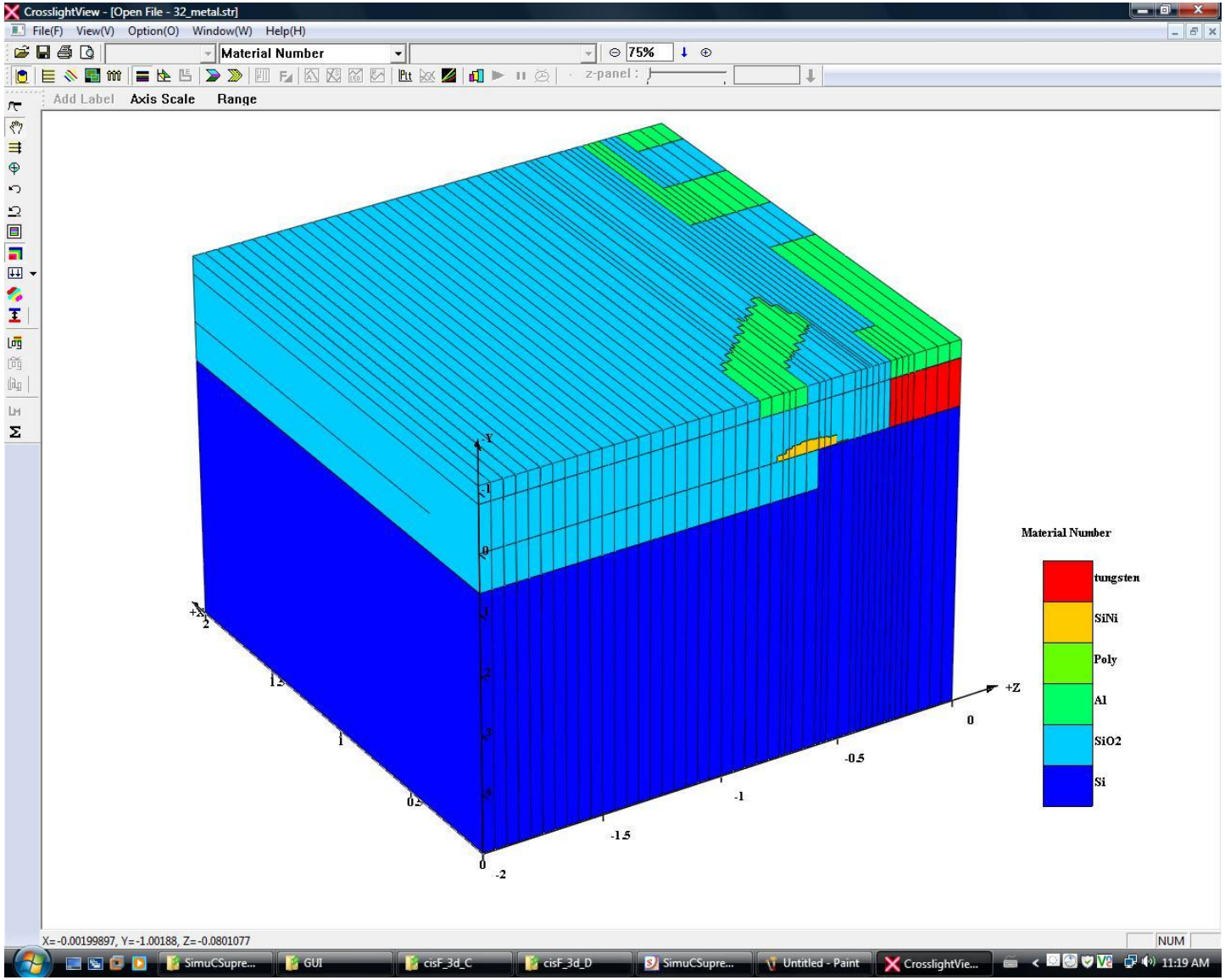
ILD1 and Contact holes (mask set 07)



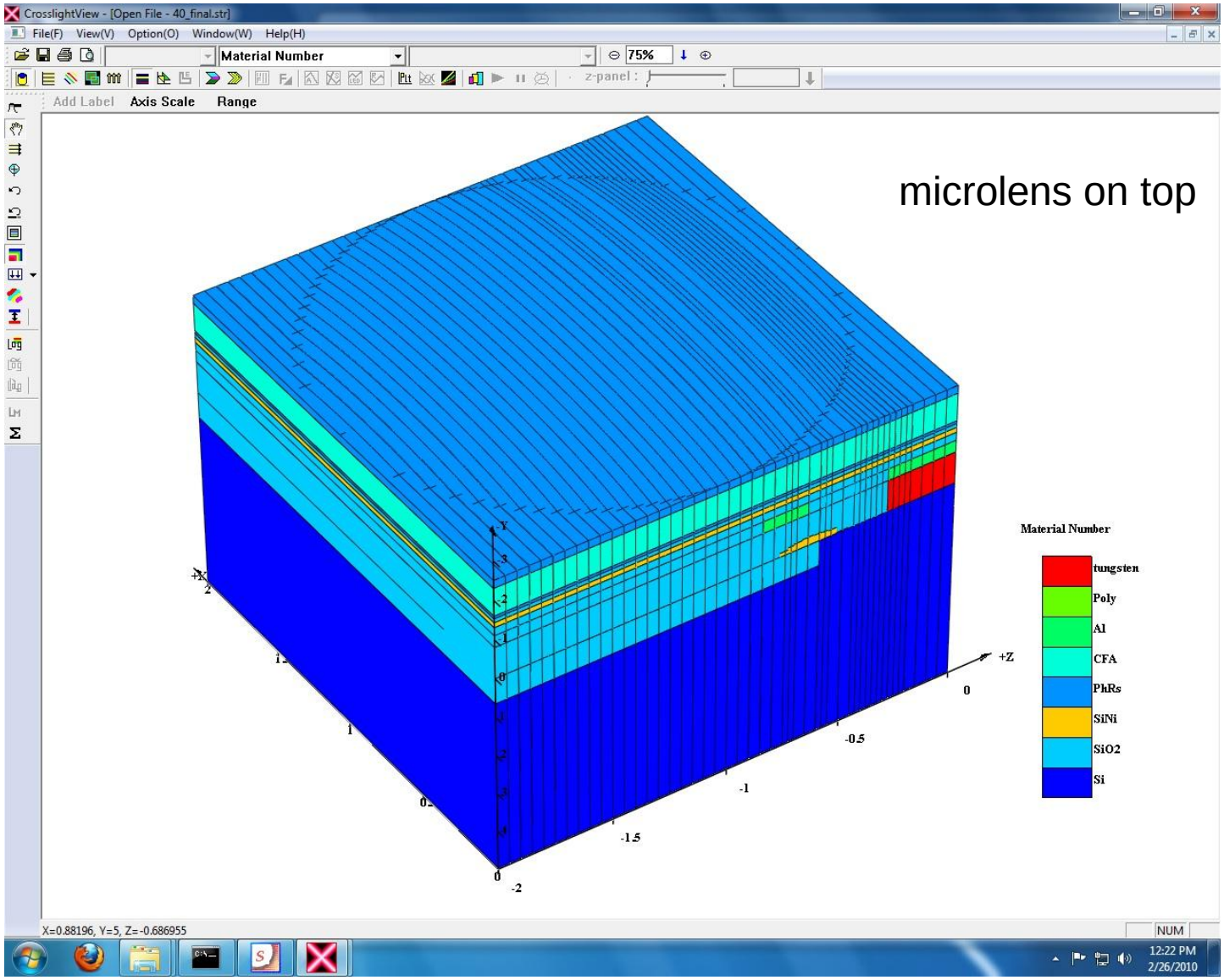
Mask Set 08 – Metal1



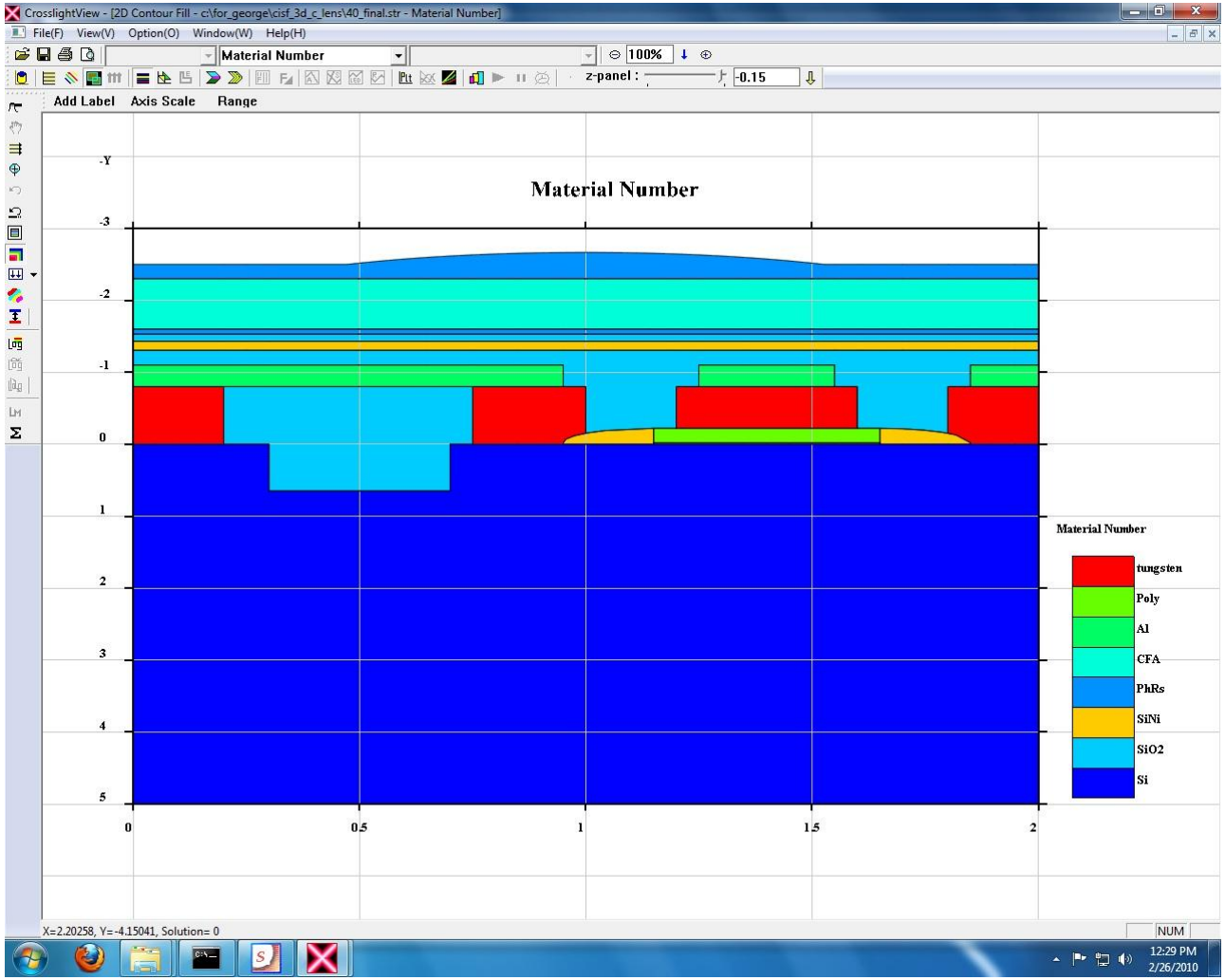
After Metal1 CMP



Structure after micro lens process

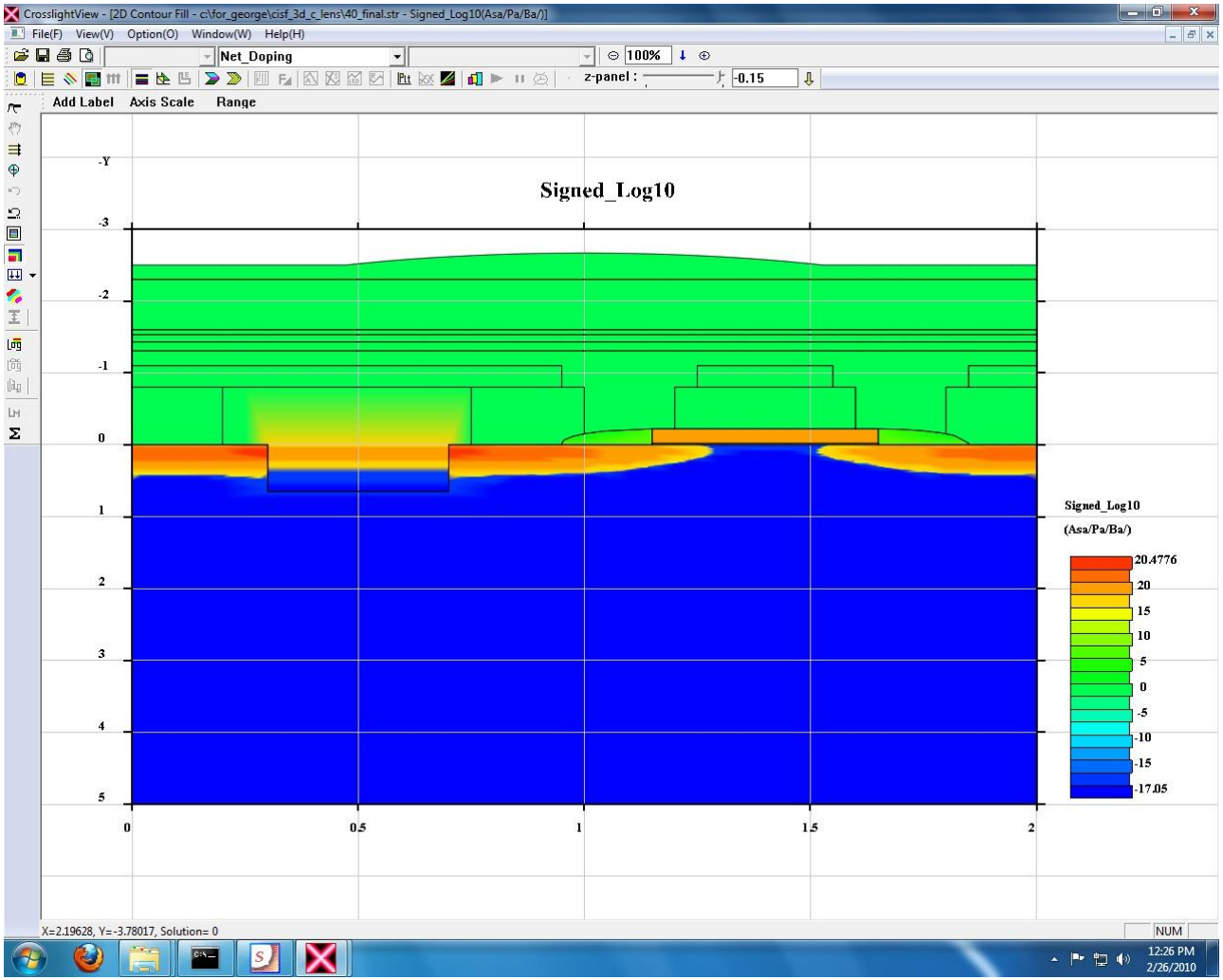


Structure – 2D cut



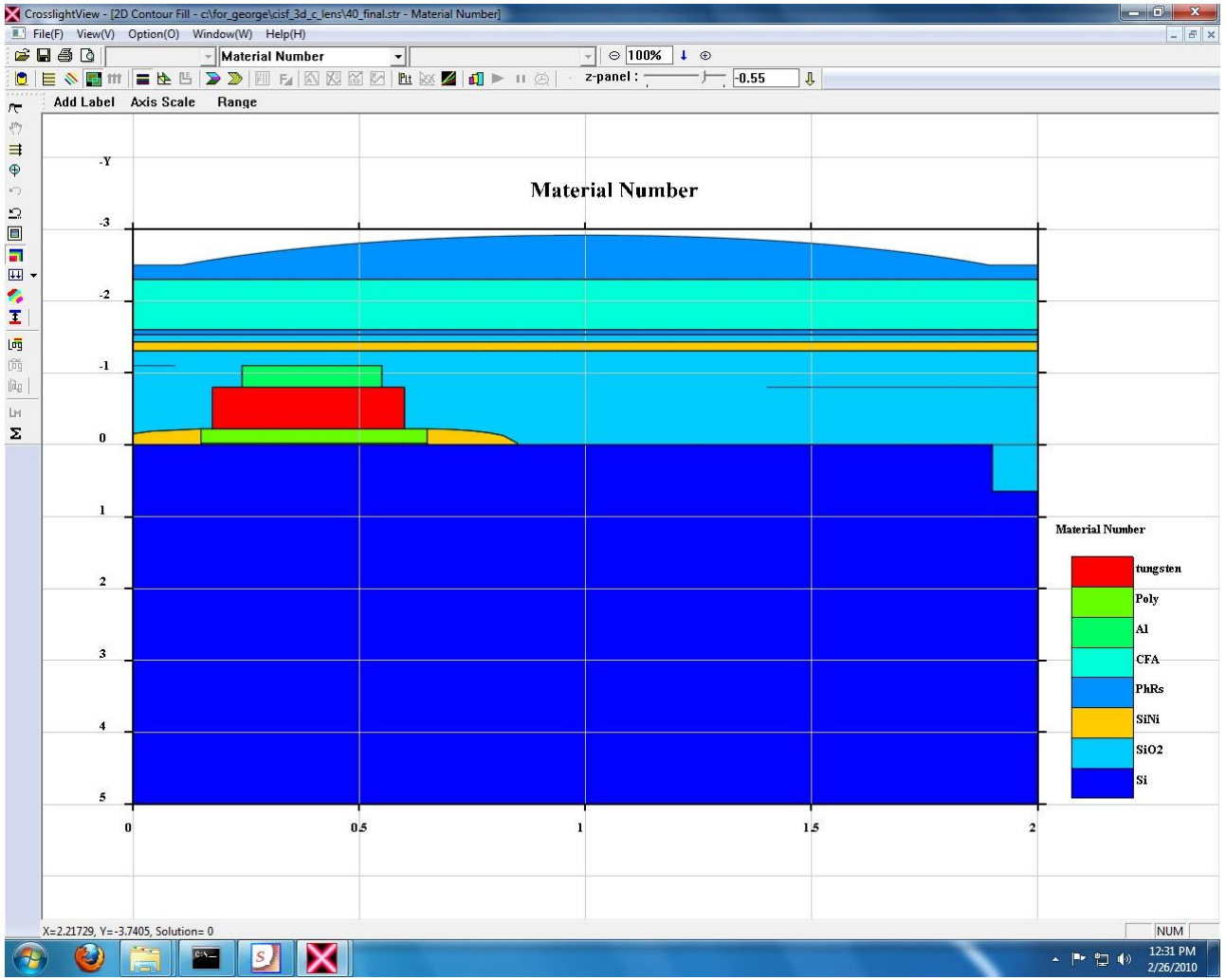
- Cut along –0.15 um (corresponding to mask set Z Axis).

Net Doping Profile – 2D cut



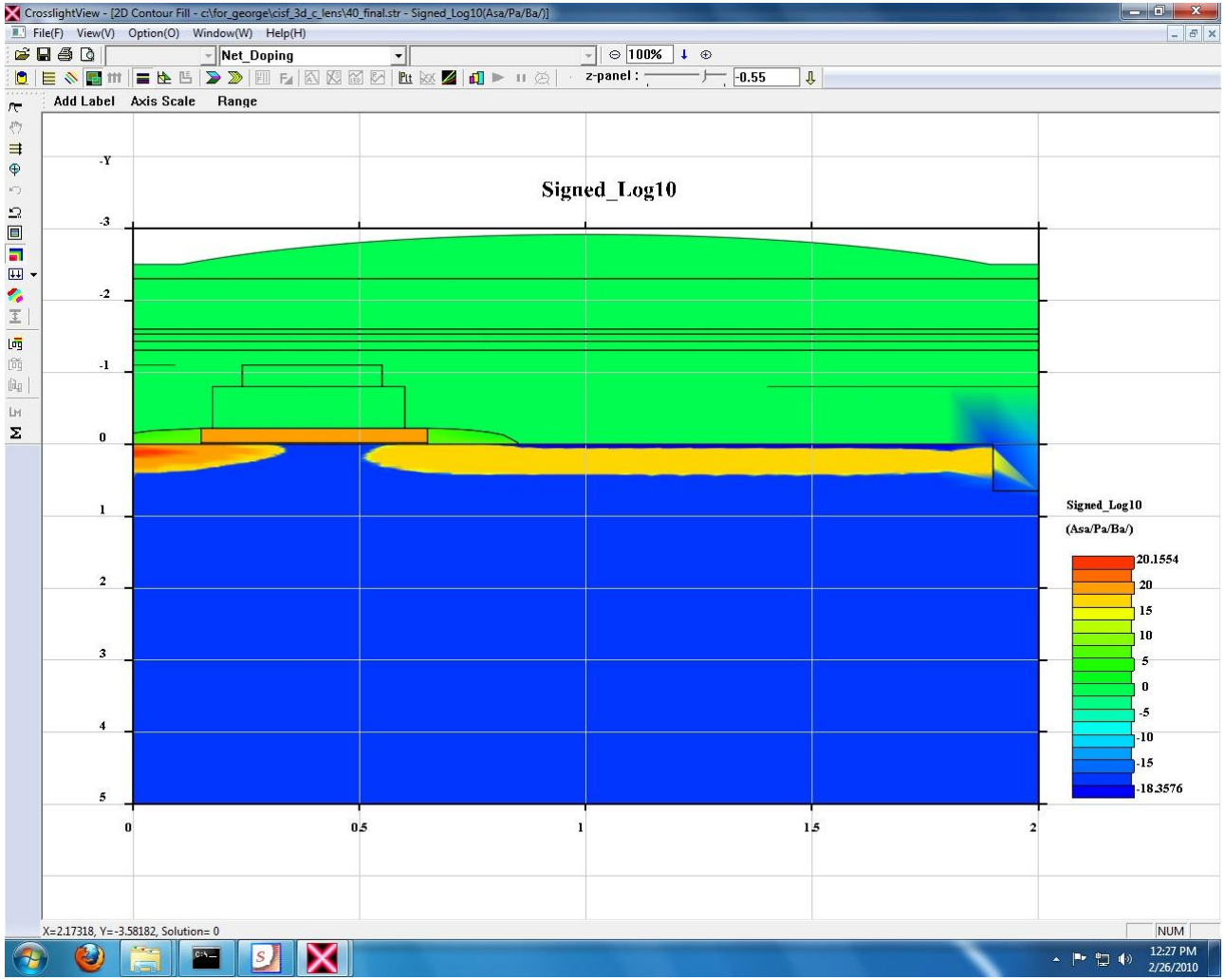
- Cut along –0.15 um (corresponding to mask set Z Axis).

Structure – 2D cut



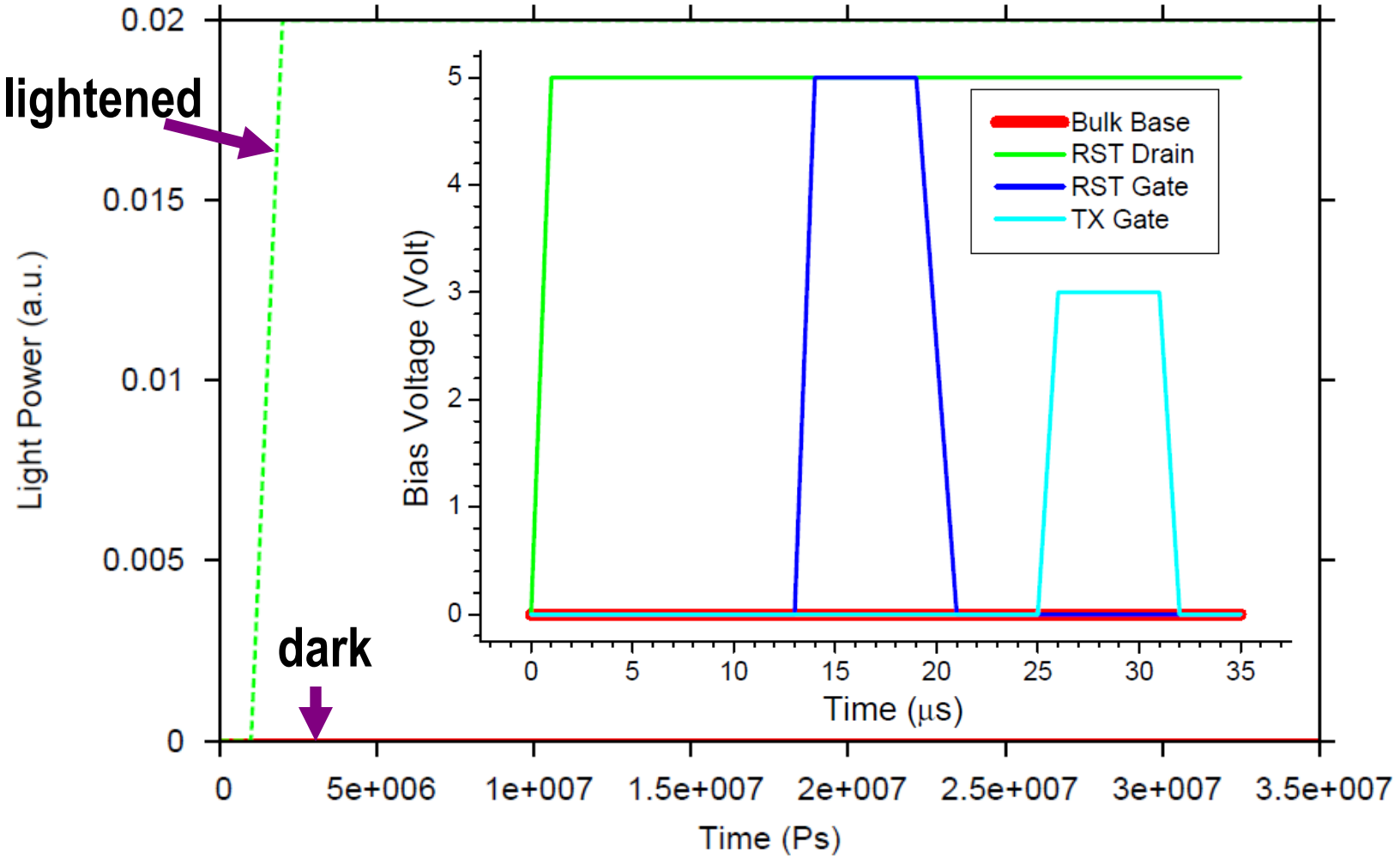
- Cut along –0.55 um (corresponding to mask set Z Axis).

Net Doping Profile – 2D cut



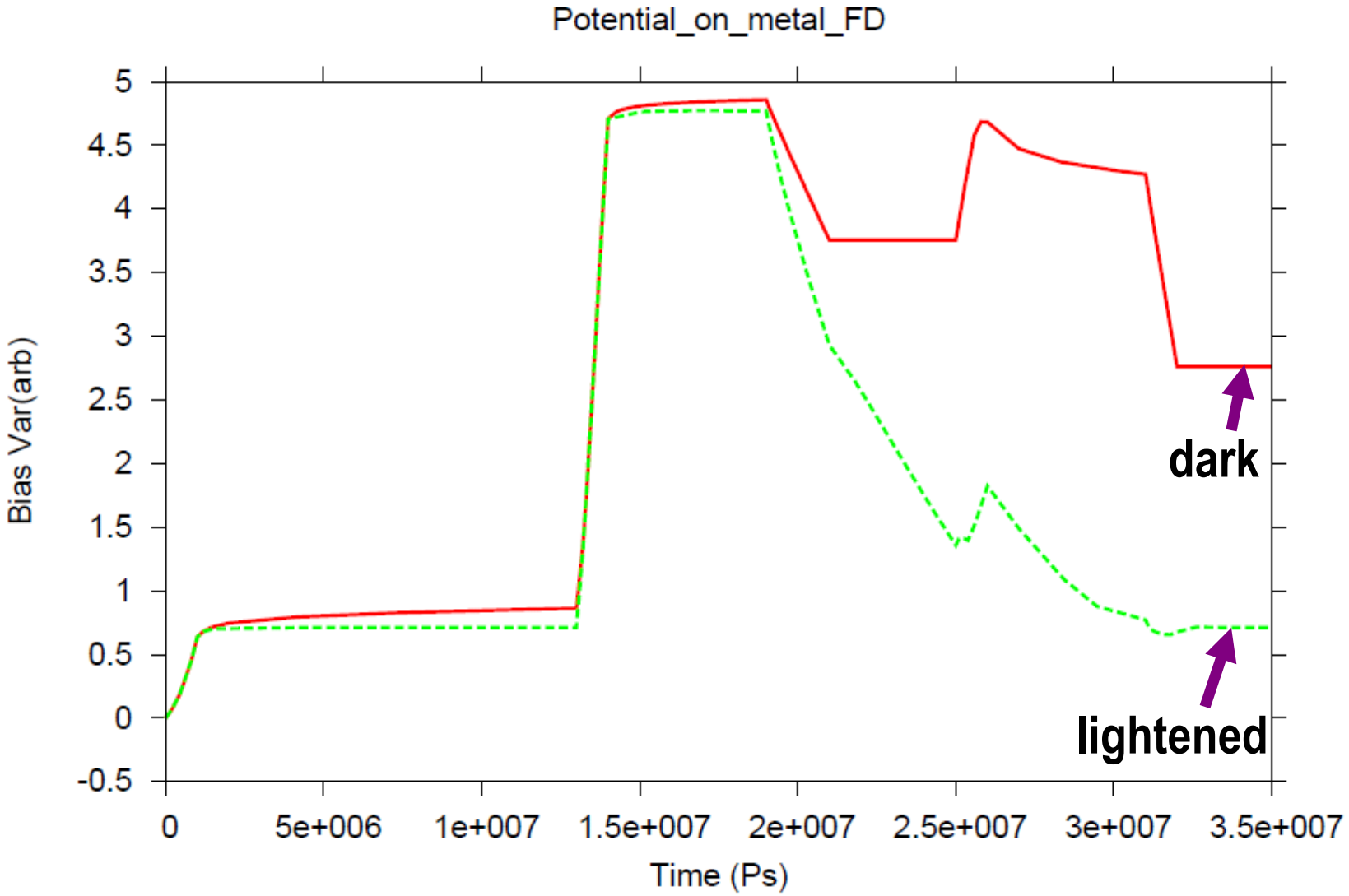
- Cut along –0.55 um (corresponding to mask set Z Axis).

Bias Clocking

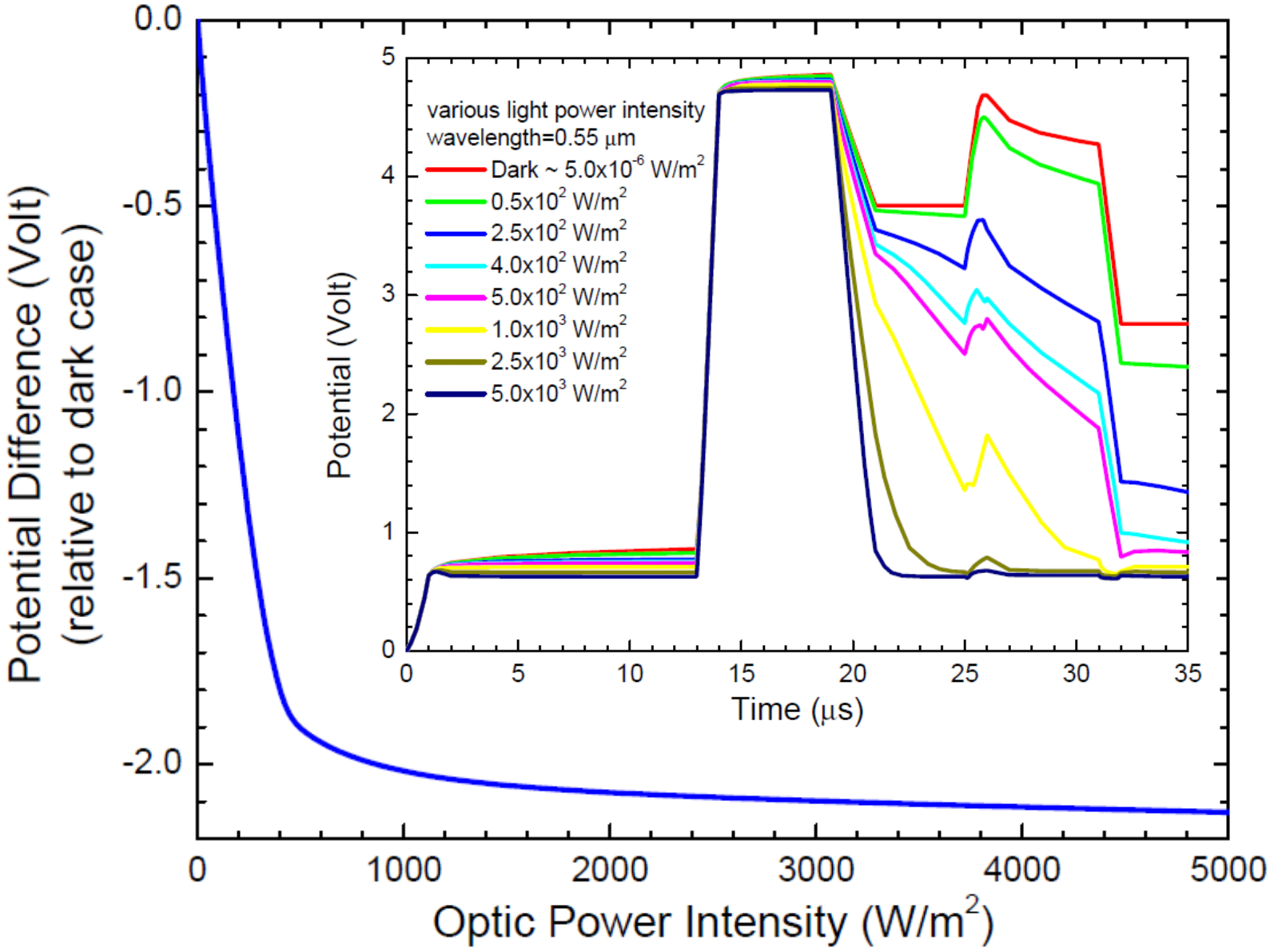


- Light power base unit is 5×10^4 W/m^2.

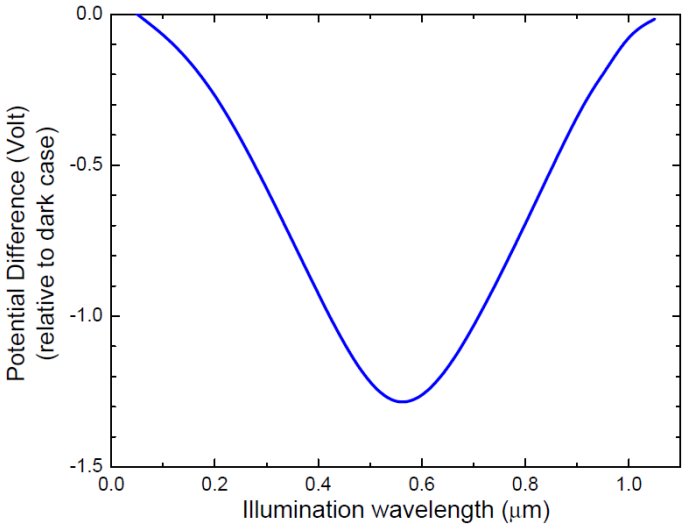
Results – Potential Comparison

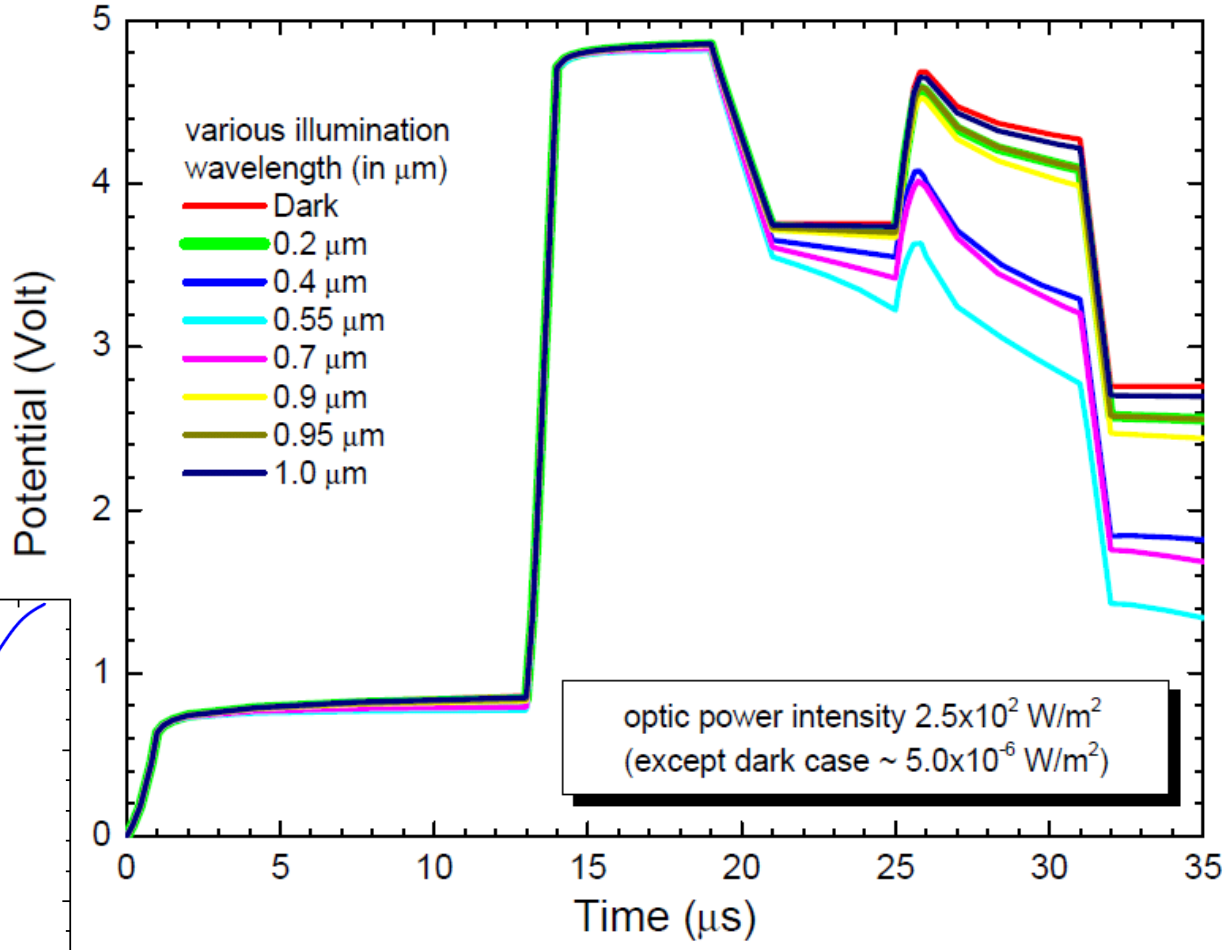


Results – Potential Difference vs. Optic Power

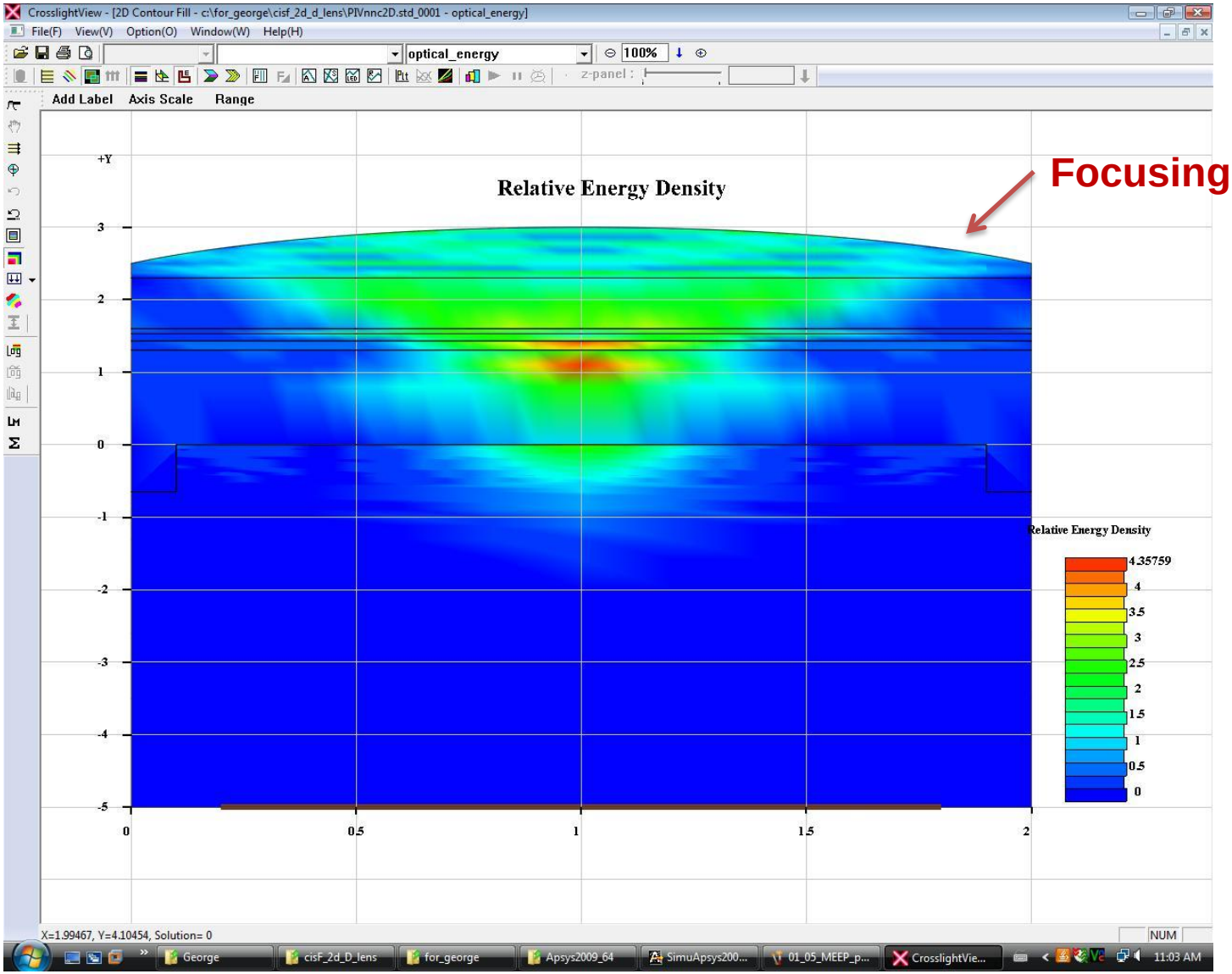


Results – Potential Difference vs. Wavelength





Initial Results for 2D FDTD Simulation with Lens



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