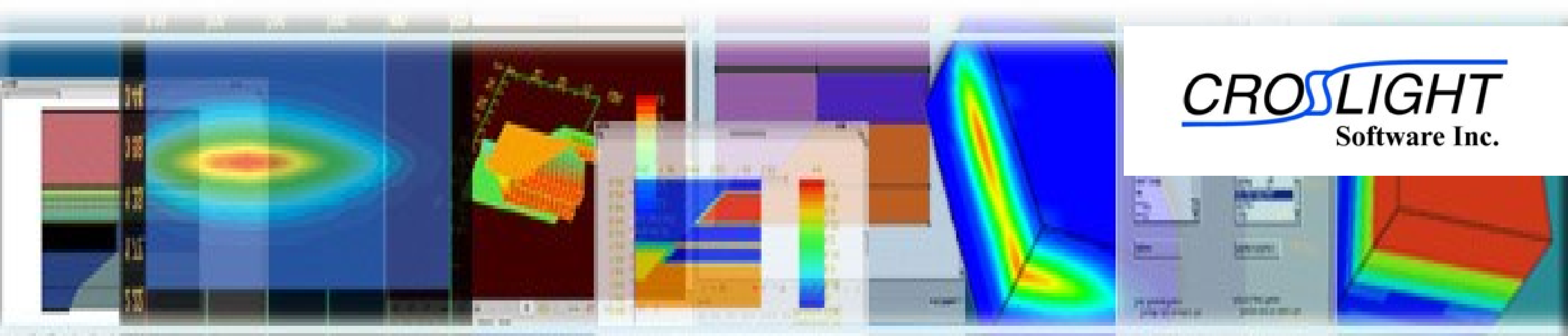
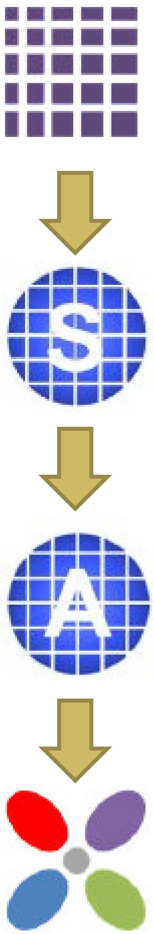


Lighting Up Semiconductor World…

APSYS | CSUPREM | LASTIP | PICS3D | PROCOM | CROSSLIGHTVIEW

3D Simulation of SOI FinFET

Simulation Flows of SOI FinFET



MaskEditor is a one step 2D/3D layout designer. It can read the user generated GDSII files and prepare the masks for the CSUPREM process simulator.

CSUPREM is the next generation 2D/3D process simulator. SimuCSUPREM is the graphic user interface for CSUPREM with rich features like Design of Experiment (DOE), real time wizard, etc.

APSYS is an advanced device simulation tool. SimuAPSYS is the graphic user interface for APSYS with rich features like DOE, real time wizard, etc.

CrosslightView is a powerful and easy to use plotting GUI for both process and device 2D/3D simulations. It allows user to view all the physical parameters as well as I-V curves.

Introduction to MaskEditor

What's MaskEditor?

A powerful 3D mask editing tool for 3D process simulation.

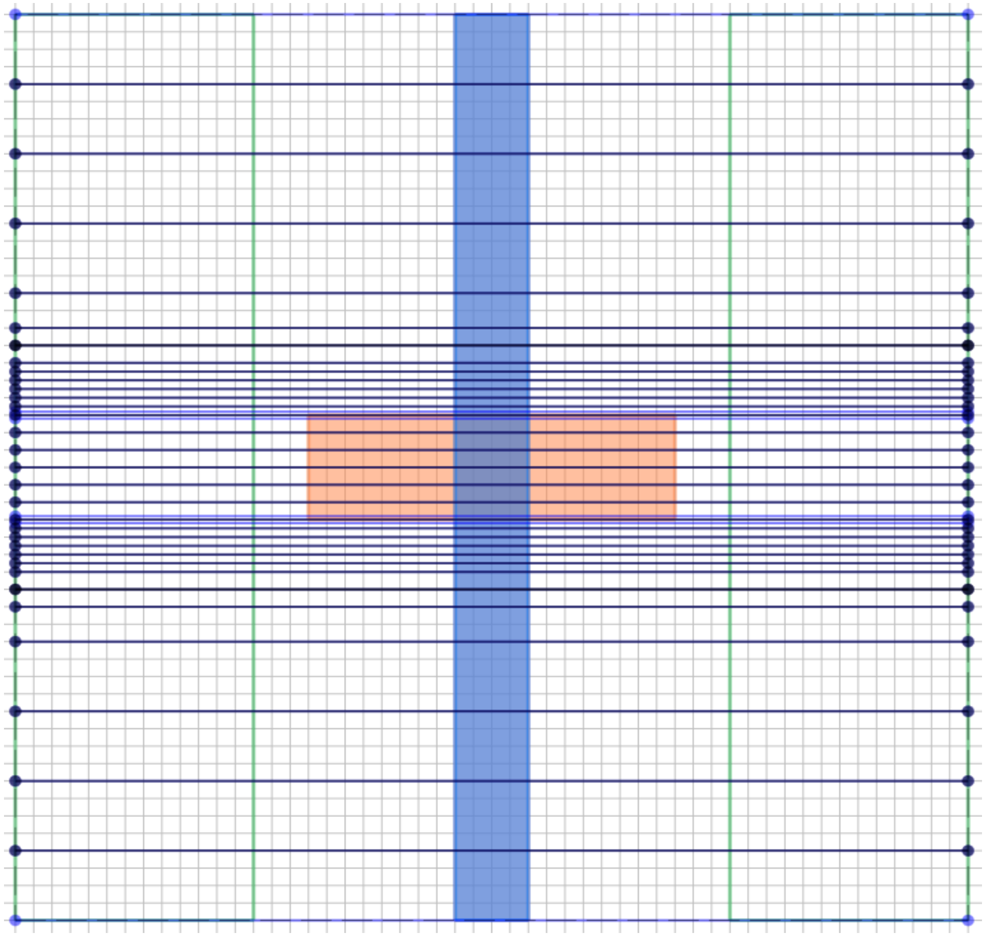
What are the Applications?

- MaskEditor is a general purpose layout tool .
- Works seamlessly with CSuprem to create 3D structure for virtually all types of semiconductor devices, like MOSFET, BJT, LED, etc.

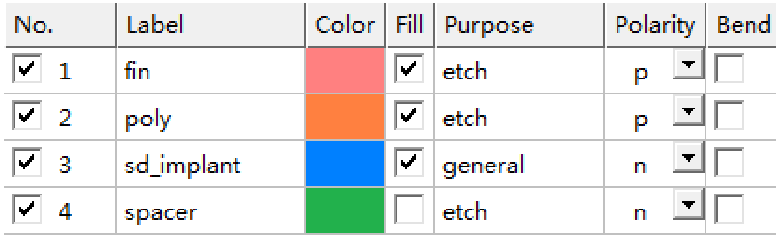
What are the Basic Functions of MaskEditor?

- Creates device layout files in GDSII format from scratch.
- Auto cutting and generate masks needed for 3D Csuprem process simulation.

Masks for SOI FinFET by MaskEditor



Four masks are used here.



No.	Label	Color	Fill	Purpose	Polarity	Bend
☑ 1	fin	🟥	☑	etch	p	☐
☑ 2	poly	🟧	☑	etch	p	☐
☑ 3	sd_implant	🟦	☑	general	n	☐
☑ 4	spacer	🟩	☐	etch	n	☐

Label: to give a label of this mask.
Purpose: to define the purpose of this mask. If it’s “etch” this mask will be used for etching some material. If it’s “general”, this mask will be used for implanting.
Polarity: to define the polarity of the photoresist, negative or positive.

CROSSLIGHT Software Inc.

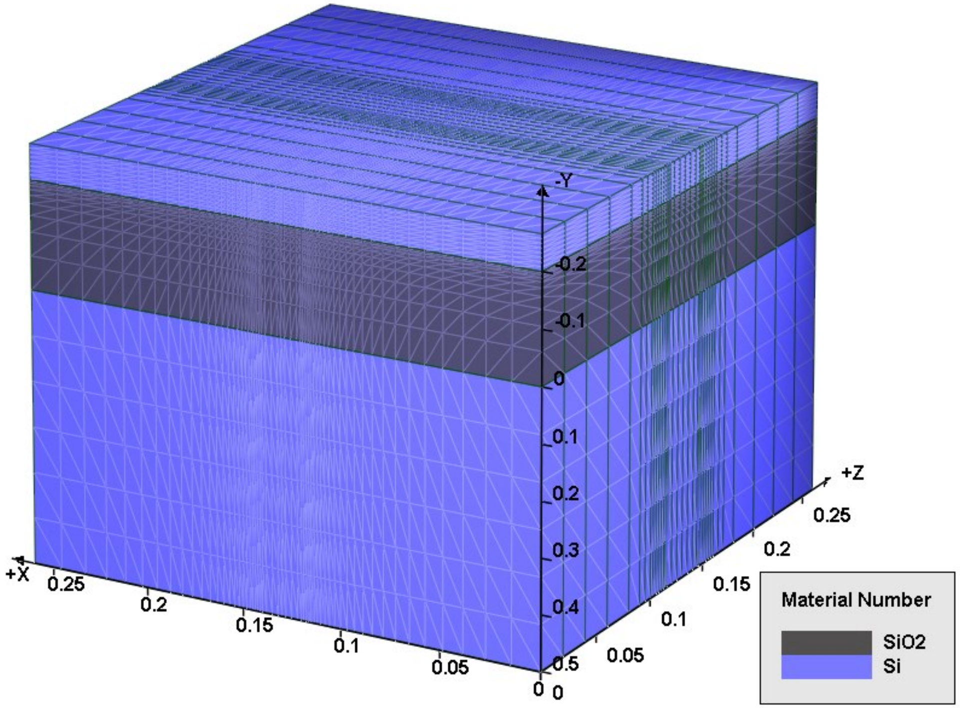
Introduction to CSUPREM

- Extension of Stanford’s code to full 3D with inter-plane coupling.
- Direct use of existing 2D input decks in 3D simulation.
- Full 3D model for implantation, diffusion, segregation & oxidation.
- Direct conversion of GDSII file into 3D simulation input decks.
- Full 3D simulation for mechanical stress.
- Flexibility of switching between quasi-3D and full-3D modes

according to speed/accuracy requirements.

Fabrication of SOI FinFET by CSUPREM

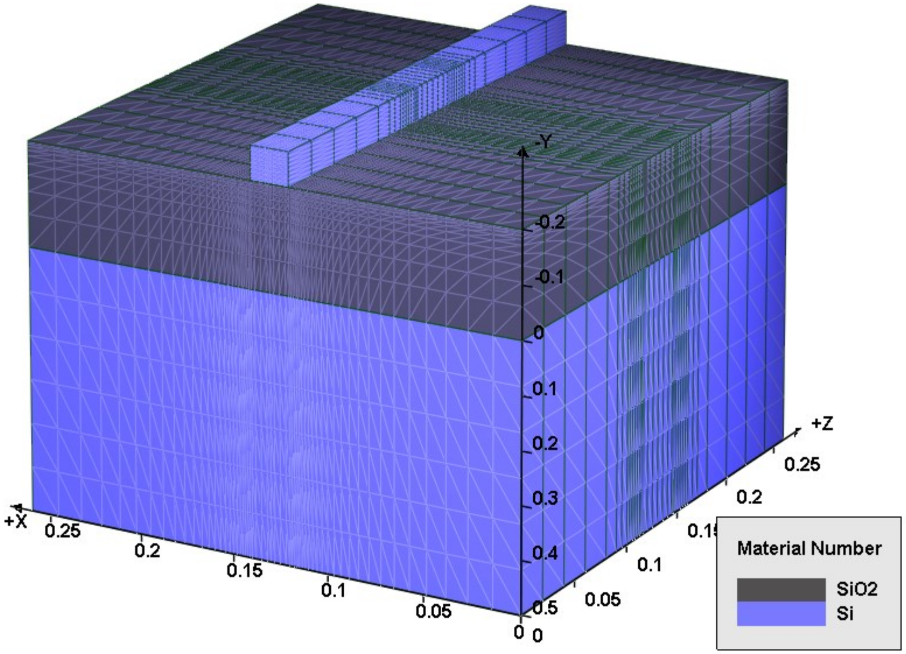
Step one: SOI Substrate



Width: 0.26um
Height: 0.26um
Silicon Substrate Thickness:0.5um
Oxide Thickness: 0.2um
Silicon Thickness: 0.065um
boron conc=5e+017cm^{-3}

Fabrication of SOI FinFET by CSUPREM

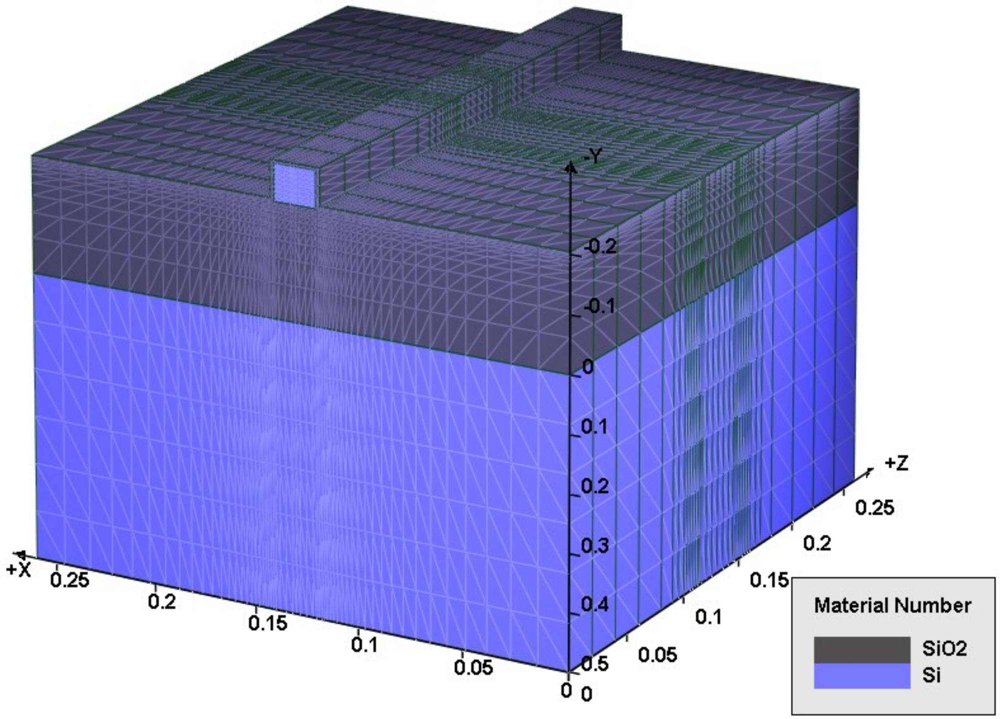
Step Two: etch fin



Width: 0.02um Height: 0.065um
Doping: boron conc=5e+017cm^{-3}

Fabrication of SOI FinFET by CSUPREM

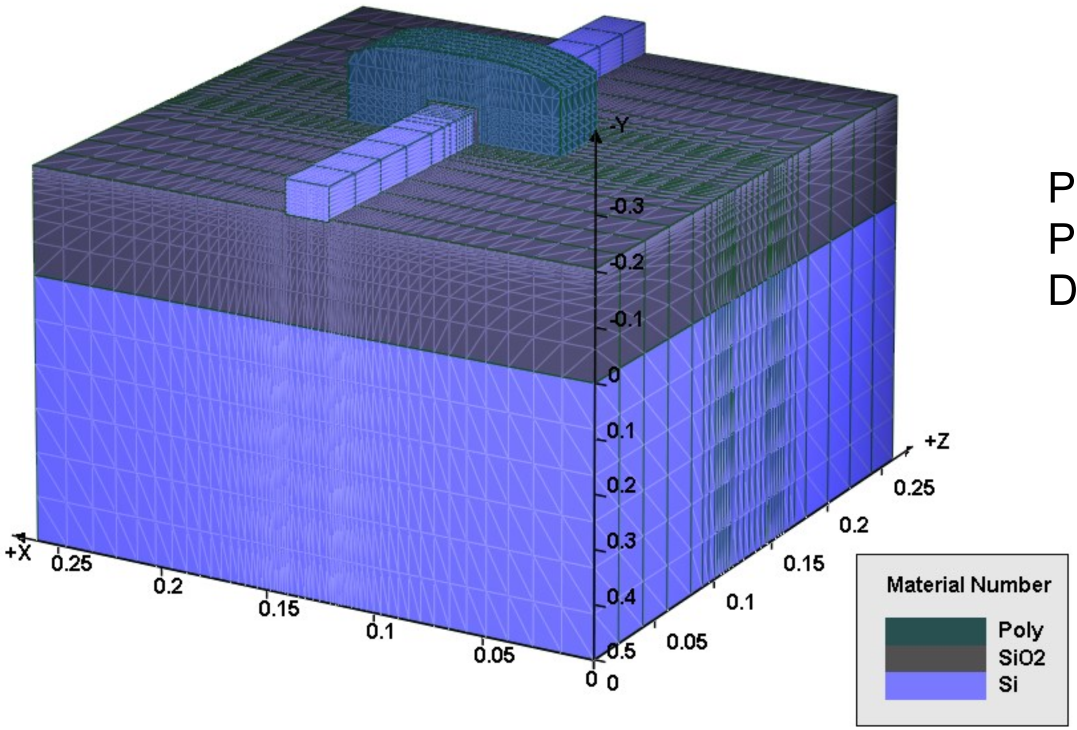
Step Three: gate oxide



Deposit and etch oxide
Gate Oxide Thickness: 0.005um

Fabrication of SOI FinFET by CSUPREM

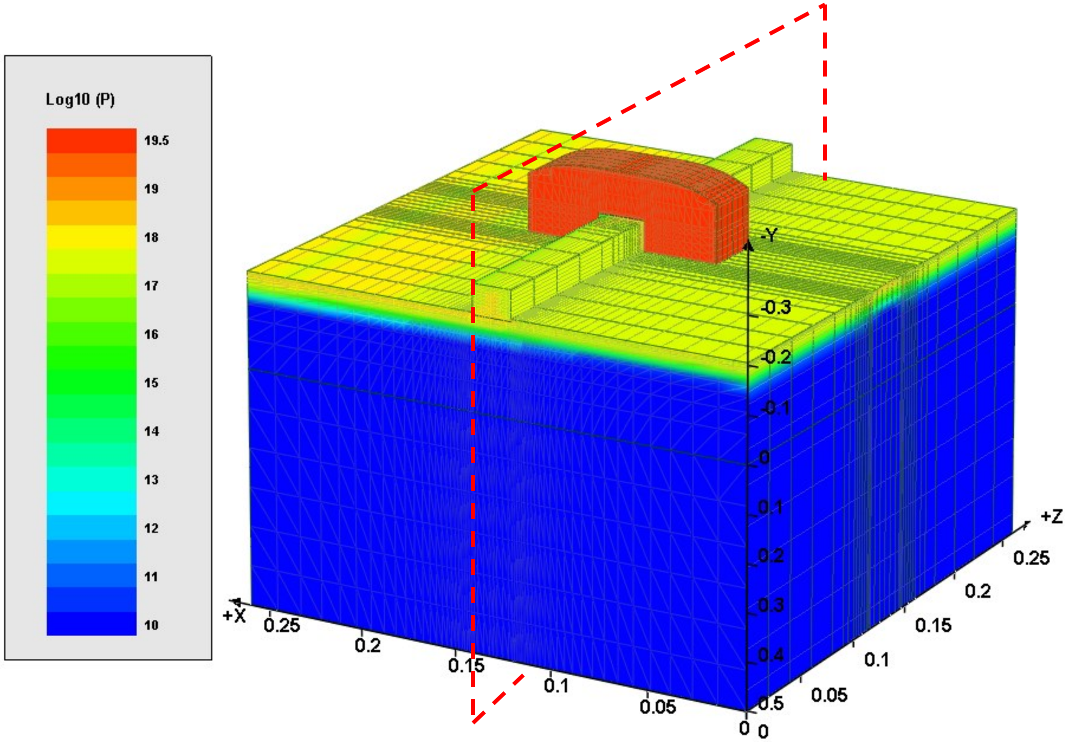
Step Four: Poly gate



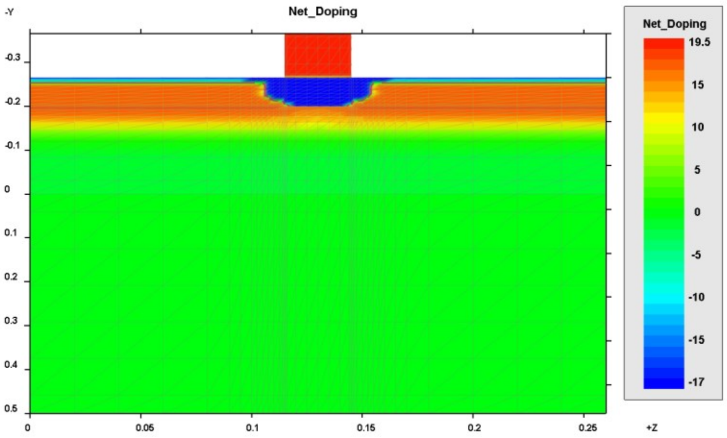
Poly Thickness:0.15um
Poly Length:0.03um
Doping: phosphorus conc=1e20cm^{-3}

Fabrication of SOI FinFET by CSUPREM

Step Five: LDD implant



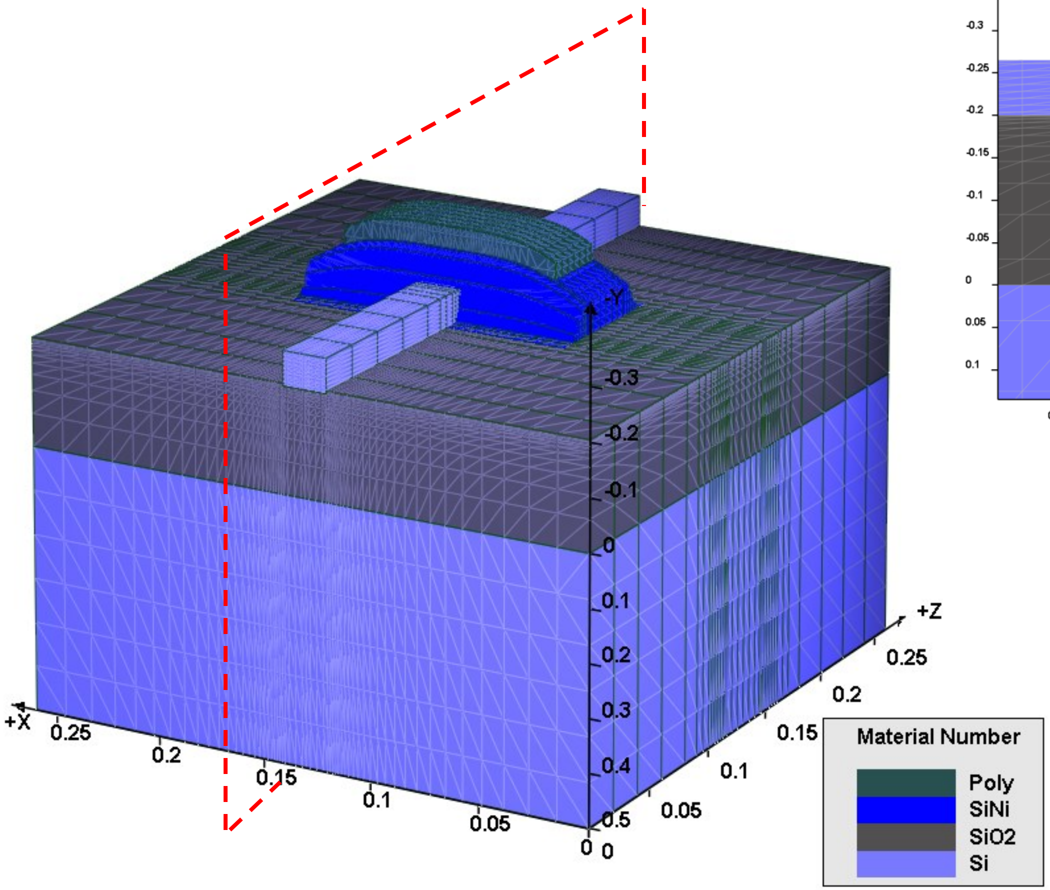
implant phosphorus
energy=10keV
Angle=60^o & -60^o
dose=1.5e+12 atoms/cm^2

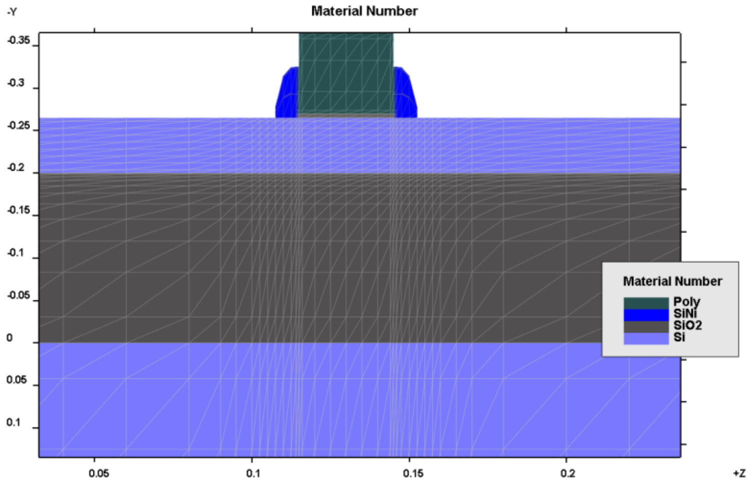


Net doping along channel

Fabrication of SOI FinFET by CSUPREM

Step Six: Spacer

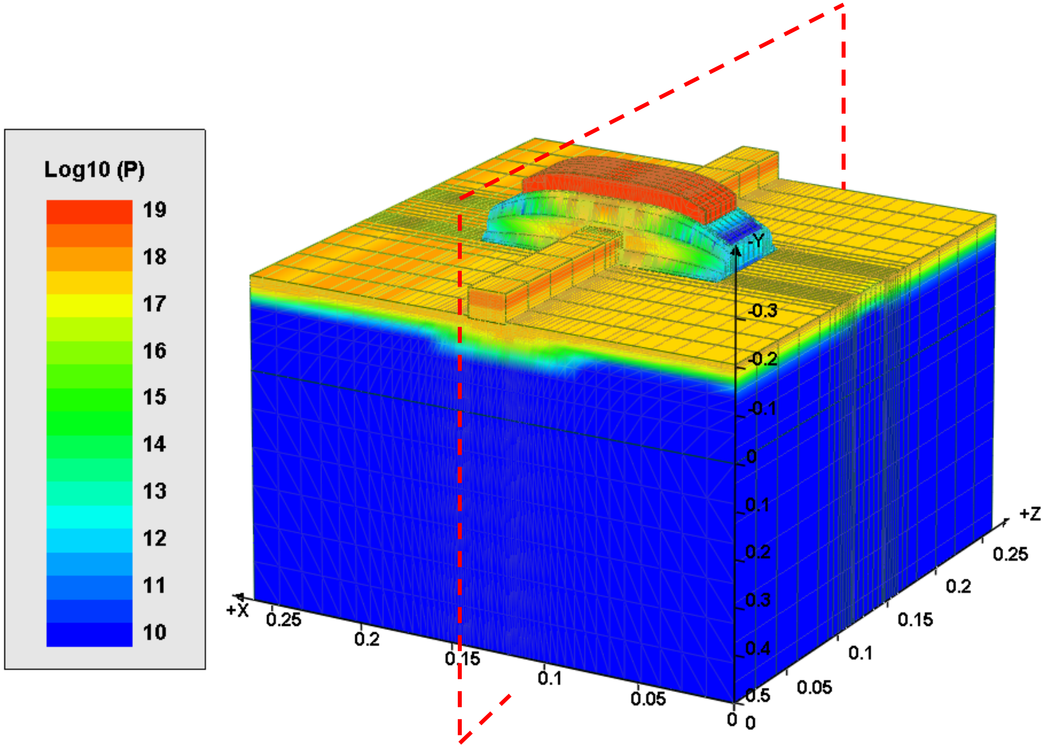




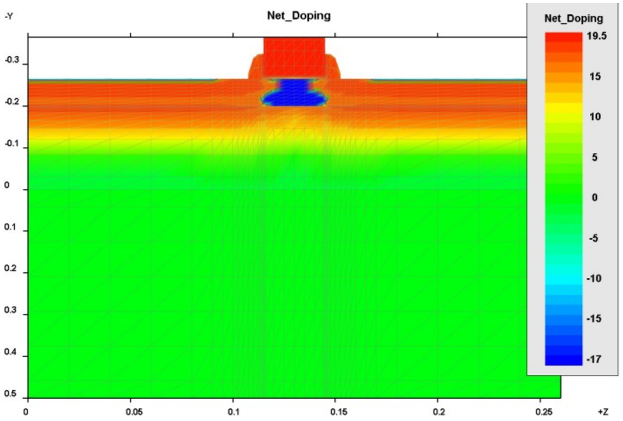
X=0.13um

Fabrication of SOI FinFET by CSUPREM

Step Seven: S/D implant



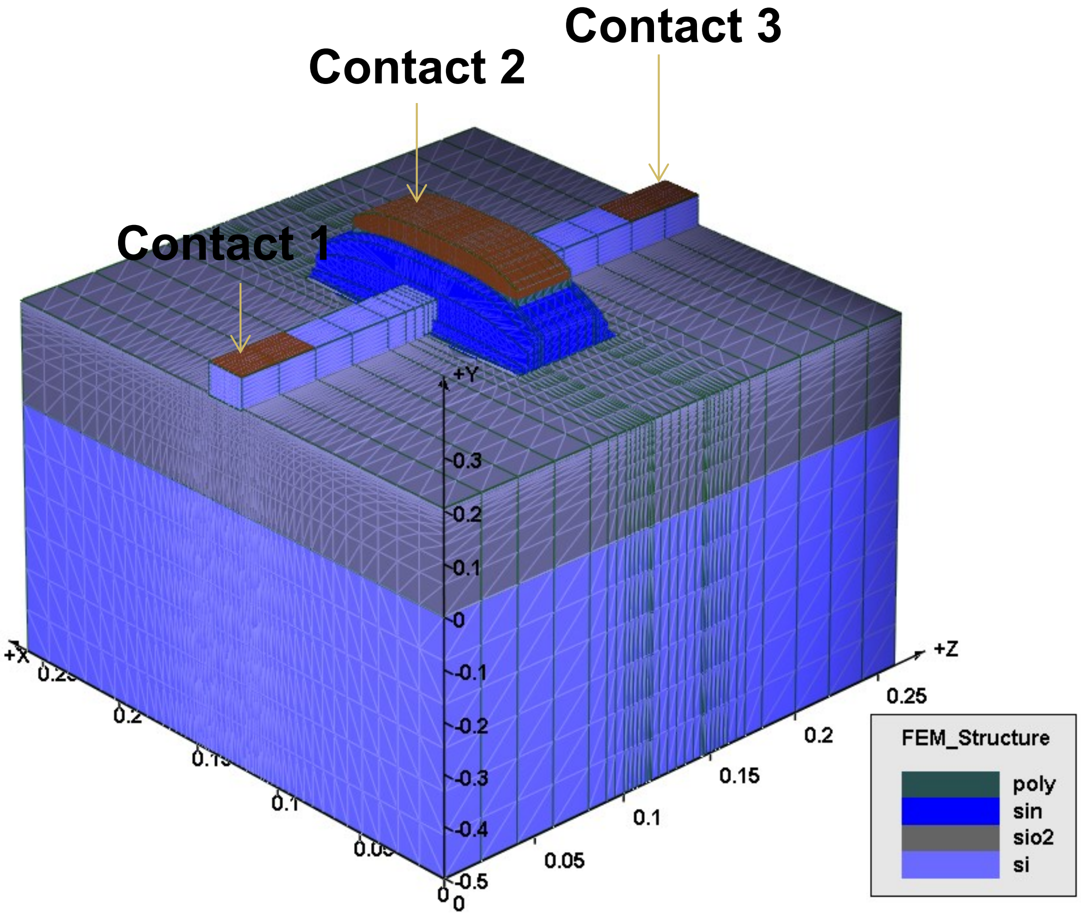
implant phosphorus
energy=15keV
Angle=0°
dose=2e+13 atoms/cm^2



Net Doping along channel

Fabrication of SOI FinFET by CSUPREM

Step Eight: Add Electrods



Contact 3

Contact 2

Contact 1

Contact 1: Source
Contact 2: Gate
Contact 3: Drain

APSYS Models for FinFET

Quantum Confinement and Oxide penestration

- 2D Schrodinger equation solved on each mesh plane perpendicular to the direction of channel.
- Separate effective masses for different band valleys of silicon taken into account for greater accuracy.
- Oxide and nitride treated as wide bandgap semiconductor material:

=> realistic potential profile for quantum confinement.

=> realistic penetration of electron wave function into oxide/nitride.

- Fast complex sparse eigen solver employed to find multiple quantum levels for each mesh plane.
- quantum wire (QWIRE, 1D) density of states (DOS) used in conjunction with the 2D wave function to generate accurate QWIRE electron spatial distribution.
- QWIRE electron density directly used in Poisson equation solution.
- QWIRE quantum levels directly used in NEGF model of ballistic current in channel.

APSYS Models for FinFET

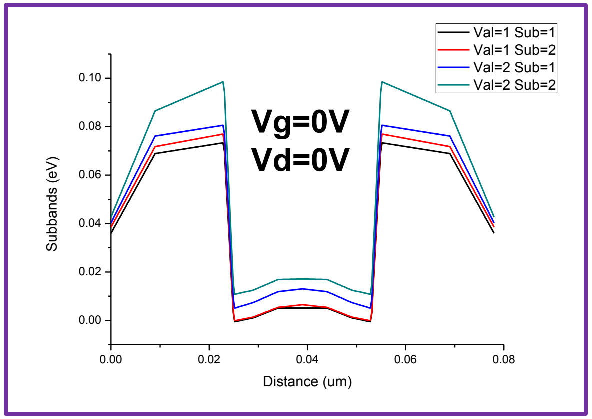
Quantum ballistic current transport model

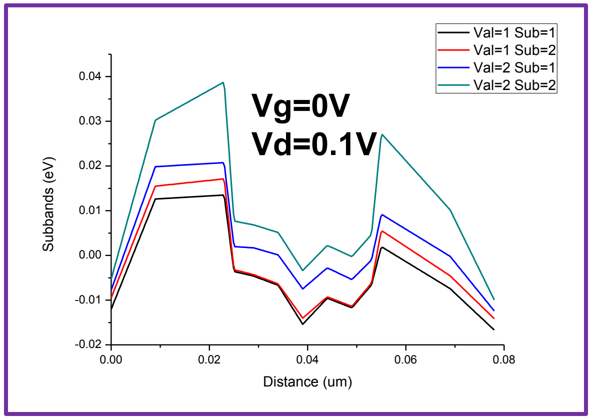
- Device divided into classical drift-diffusion (DD) regime (mainly in vicinity of contacts) and quantum ballistic transport (QBT) regime.
- NEGF model employed in QBT regime [1].
- Seamless integration of QBT and DD in the APSYS software.
- Same global Poisson's equation solver used in both DD and QBT regimes.
- Space charge from QBT model fed back into the global Poisson's equation solver to achieve self-consistency.

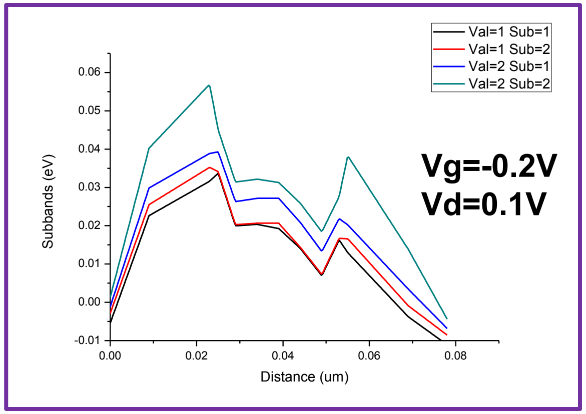
[1] *Ren, Z. (2001). "NANOSCALE MOSFETS: PHYSICS, SIMULATION AND DESIGN ".*

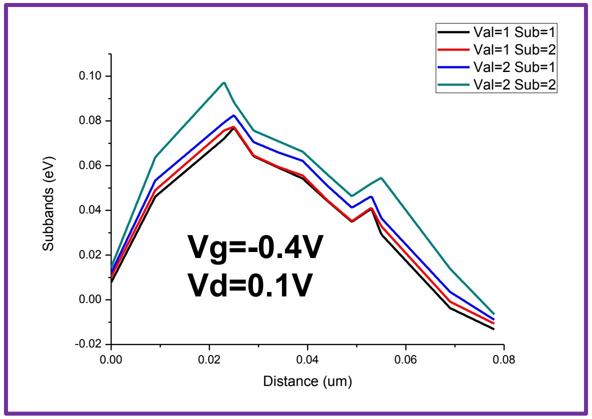
Simulation of FinFET by APSYS

Sub-bands Involved of Ballistic Transport in the Channel



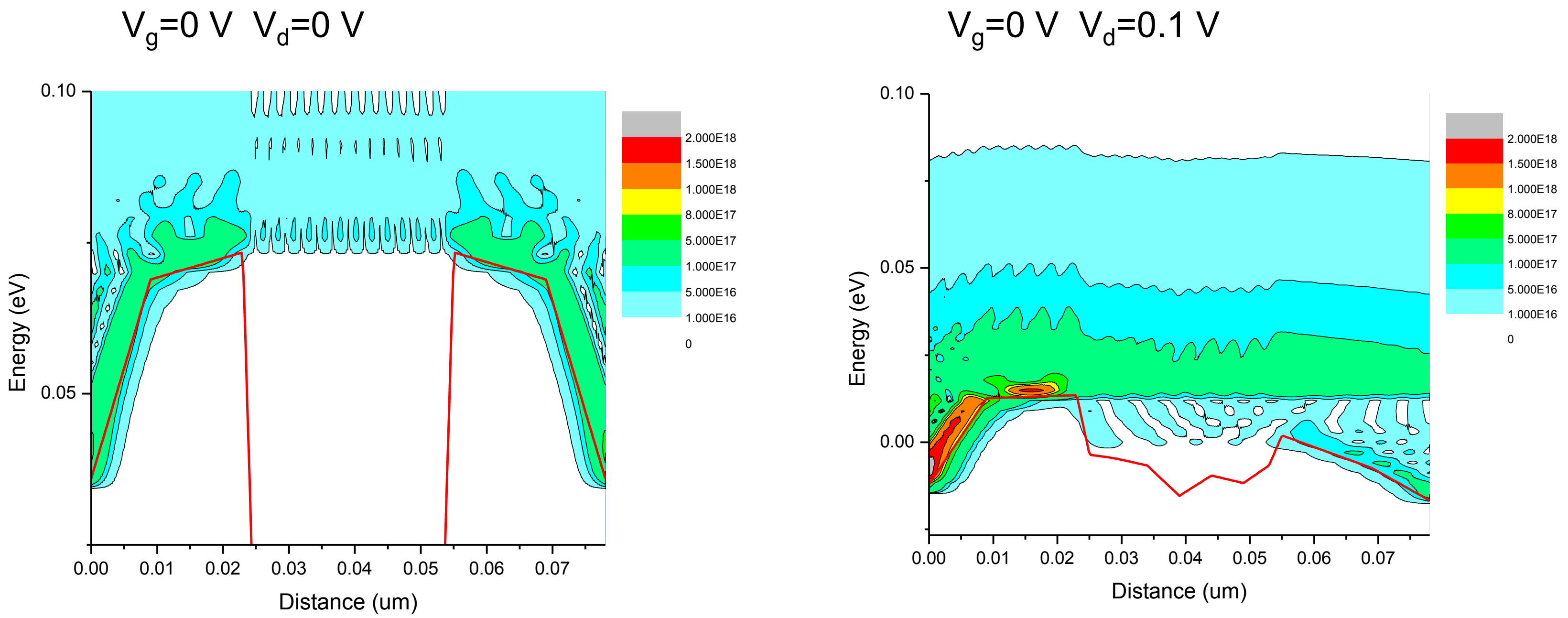






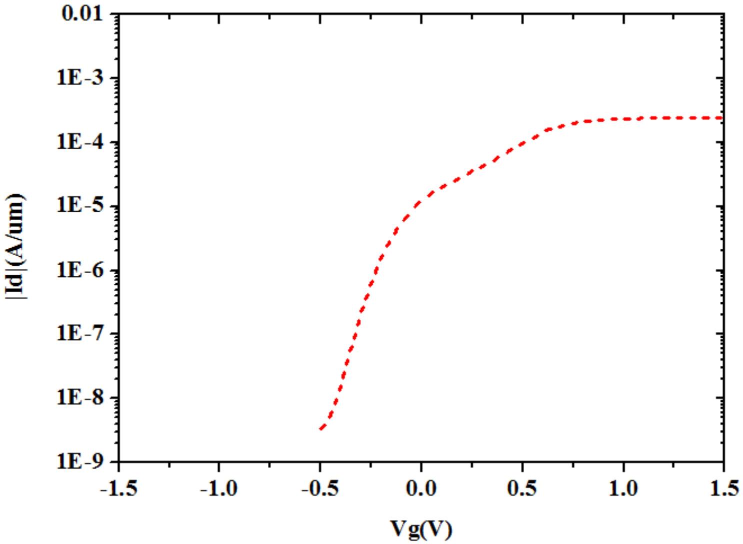
Simulation of FinFET by APSYS

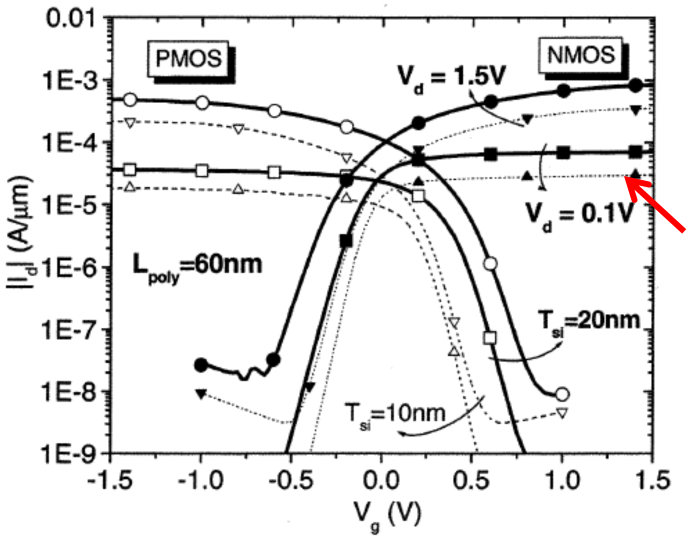
Electron Density Distribution of val=1 sub=1 along the channel

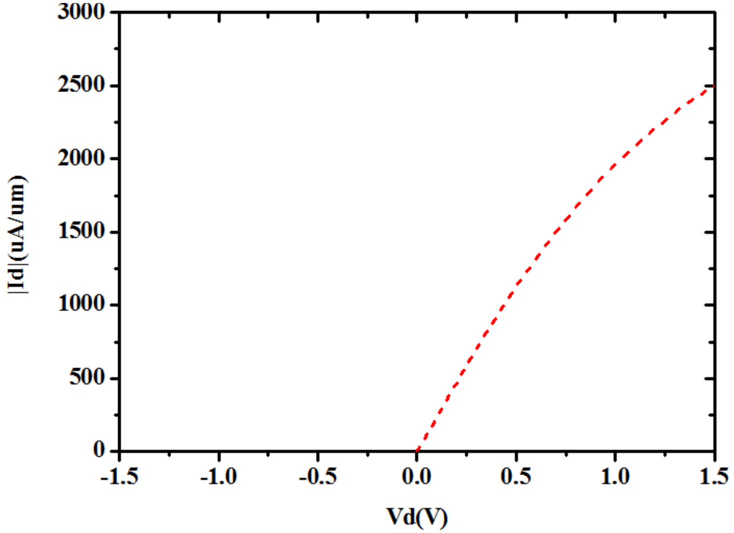


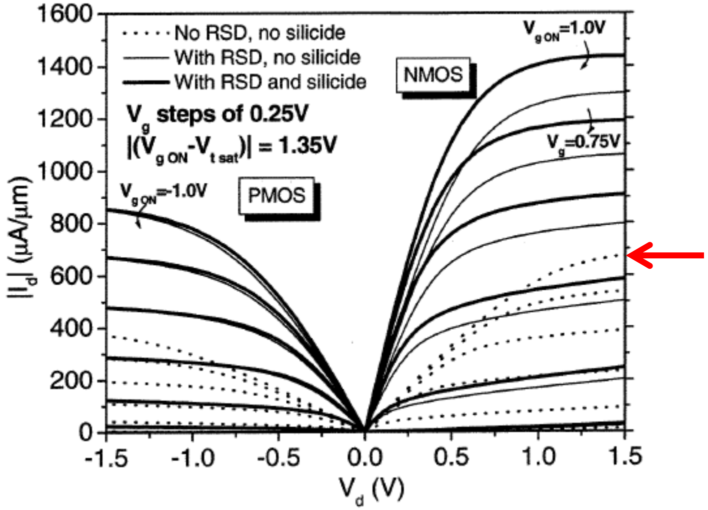
As V_d increases, more electrons will inject from source to drain by ballistic transport.

Simulation of FinFET by APSYS









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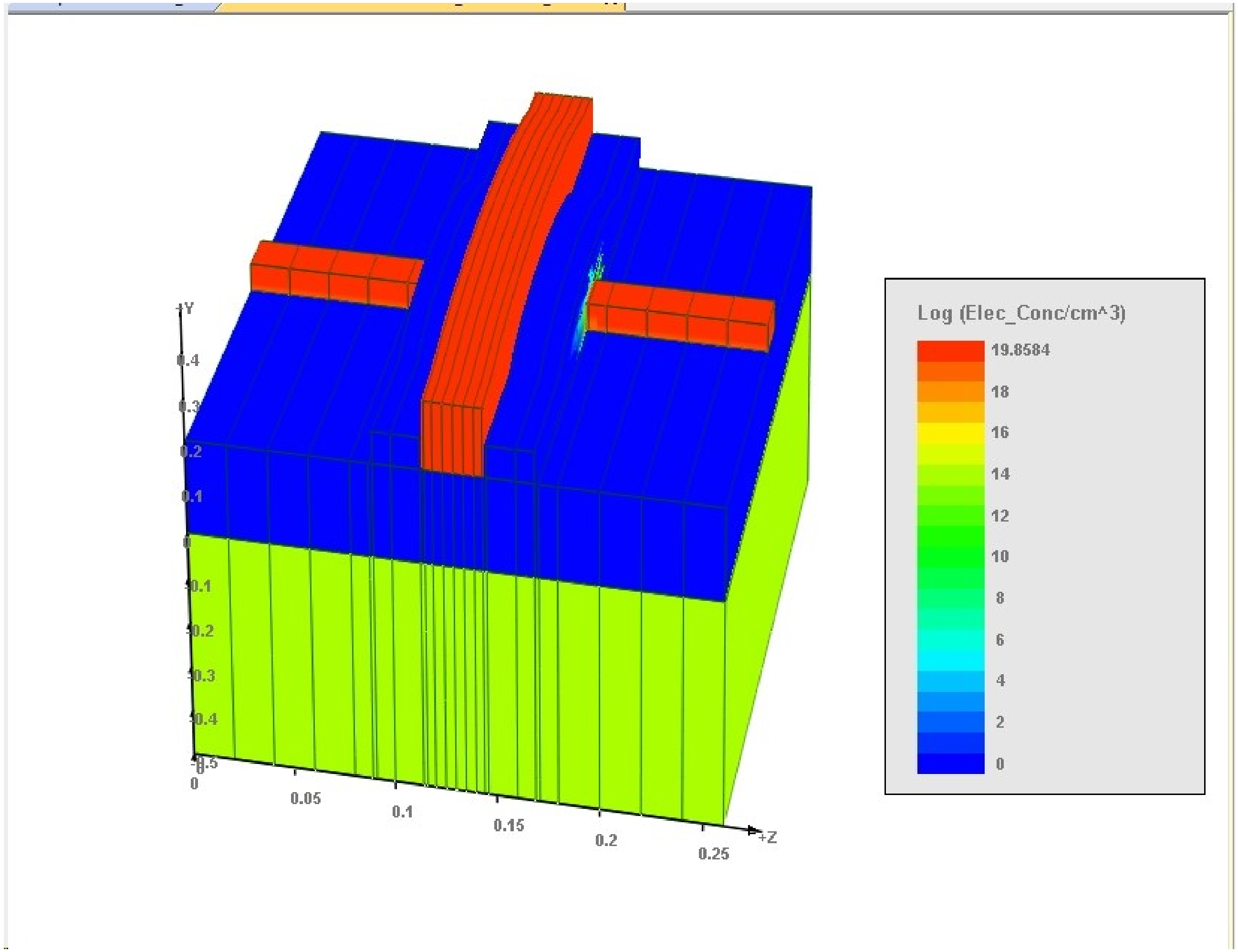
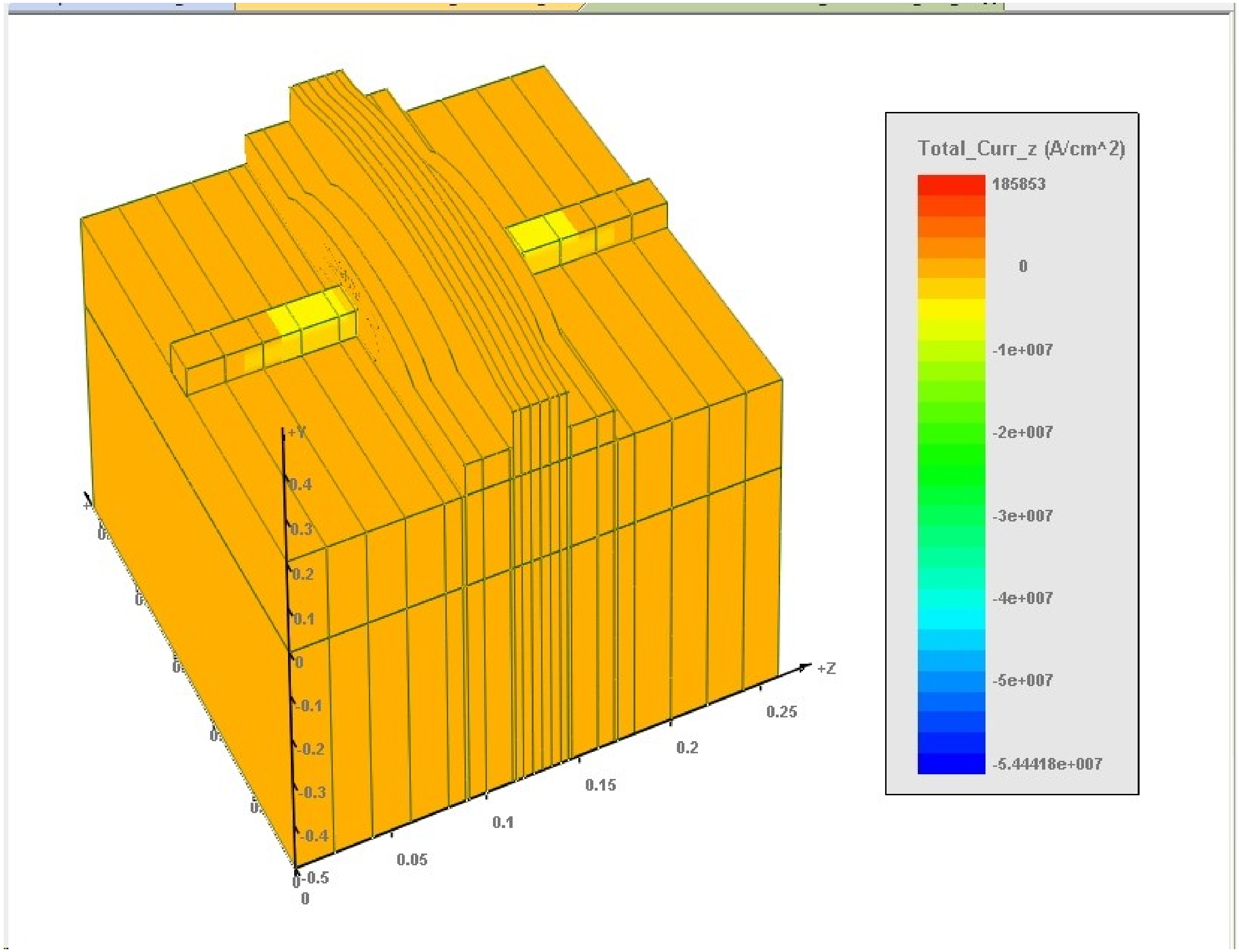
Simulation of FinFET by APSYS



Electron concentration as computed using quantum wire model with NEGF method in a self-consistent simulation. At Vg=0.1 volt and Vd=0 volt

Simulation of FinFET by APSYS



Z-component of Current flux density as computed using quantum wire model with NEGF method in a self-consistent simulation. At Vg=0.1 volt and Vd=0 volt

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