2/3D Simulation of High Voltage MOSFET

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www.crosslight.com

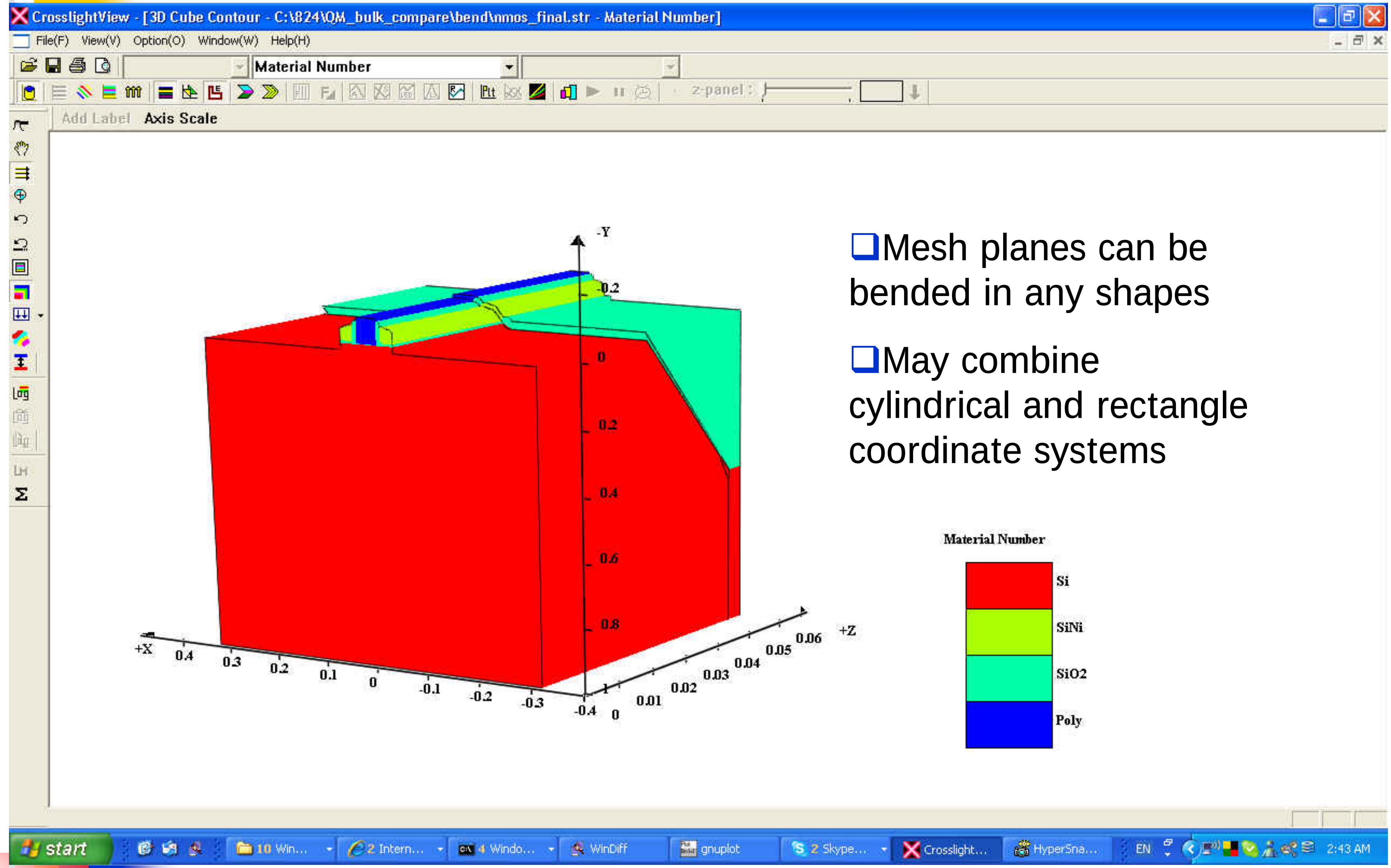
Contents

- Overview of CSuprem / Apsys models
- Process simulation
- Breakdown trend of a 300V LDMOS
- 3D Simulation with floating gates
- 3D Simulation of hybrid IGBT
- Summary

CSuprem (2/3D) -Crosslight's Advanced Process Simulator

- Extension of Stanford's code to full 3D with inter-plane coupling.
- Direct use of existing 2D input decks in 3D simulation.
- Full 3D model for implantation, diffusion, segregation & oxidation.
- Direct conversion of GDSII file into 3D simulation input decks.
- Full 3D simulation for mechanical stress, bending and vibration motions.
- Flexibility of switching between quasi-3D and full-3D modes according to speed/accuracy requirements.

Csuprem-3D –Flexible 3D mesh


CrosslightView - [3D Cube Contour - C:\824\QM_bulk_compare\bend\nmos_final.str - Material Number]

- ❑Mesh planes can be bended in any shapes
- ❑May combine cylindrical and rectangle coordinate systems

APSYS for HV MOSFET

- Temperature dependent impact ionization.
- Various vertical field dependent mobility models.
- Self-heating/thermal analysis with various types of thermal boundaries.
- Convenient transient/AC analysis suitable for various types of floating gate simulation.
- Parallel computing capability for unlimited mesh and multi-core CPU, suitable for Window64 and Linux64 OS.

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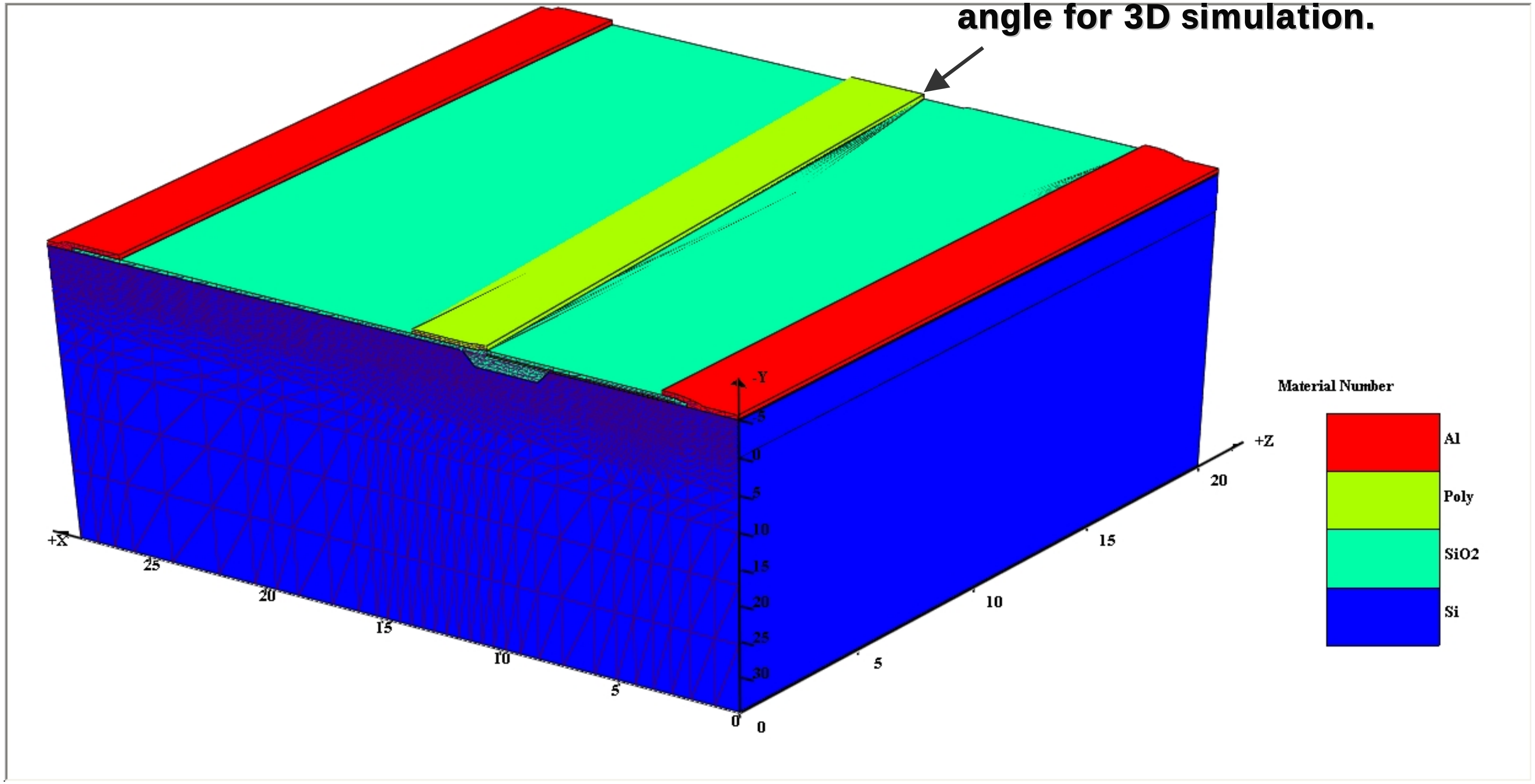
LDMOS process simulation

Key Steps

- Starting p-substrate.
- P-buried layer implant.
- N-epi layer growth.
- P-body implant.
- P-ring implant.
- Trench etching and oxide filling.
- Gate oxide and gate poly pattern
- Source/drain n+ implant.
- Vth adjust implant.
- Body contact p+ implant.
- Interfacial layer dielectric (ILD).
- Metal patterning.

2/3D device structure



Optional floating poly/metal with angle for 3D simulation.

Remark: Once 2D simulation is successful, 3D structure may be constructed using >=2 planes.

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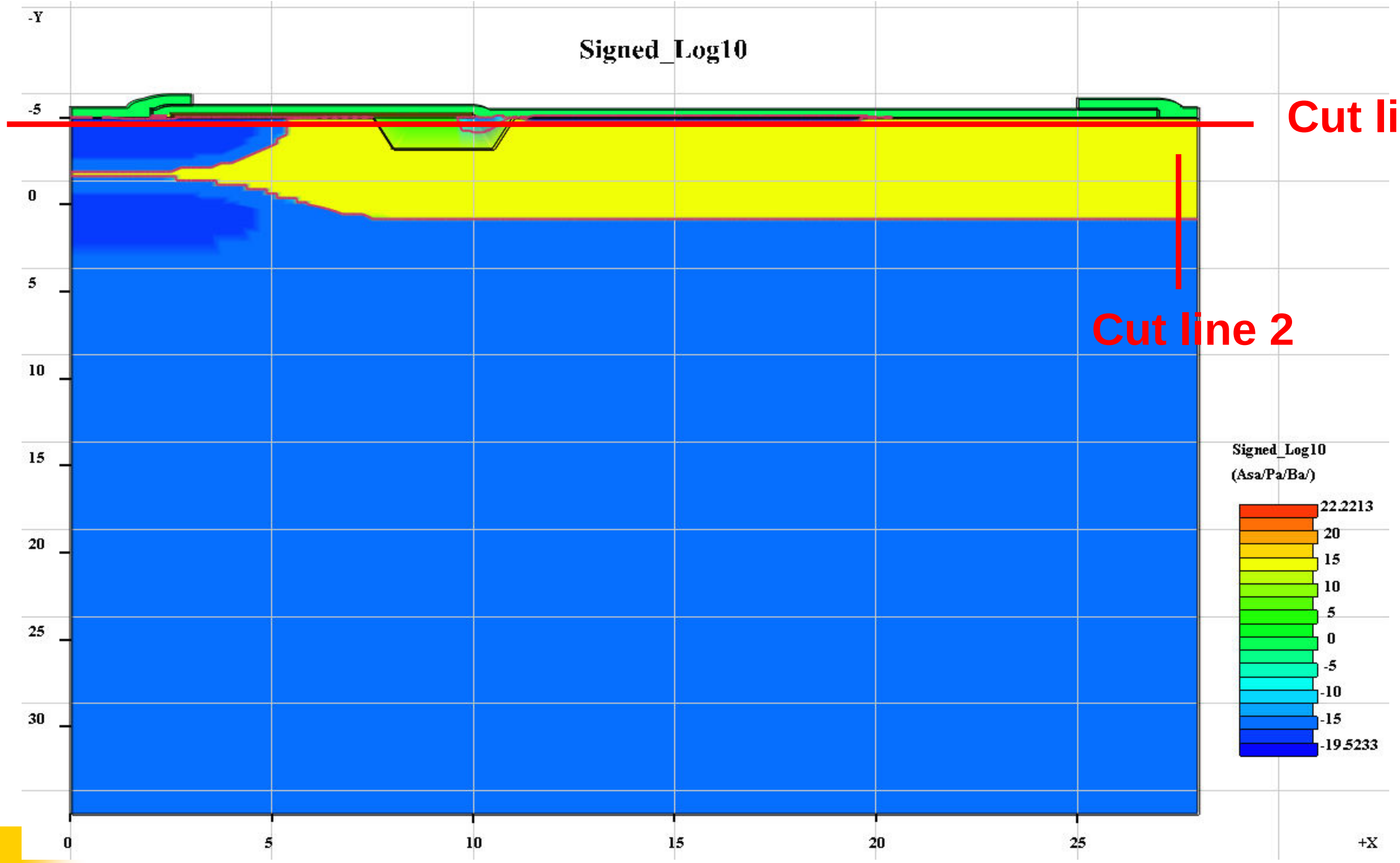
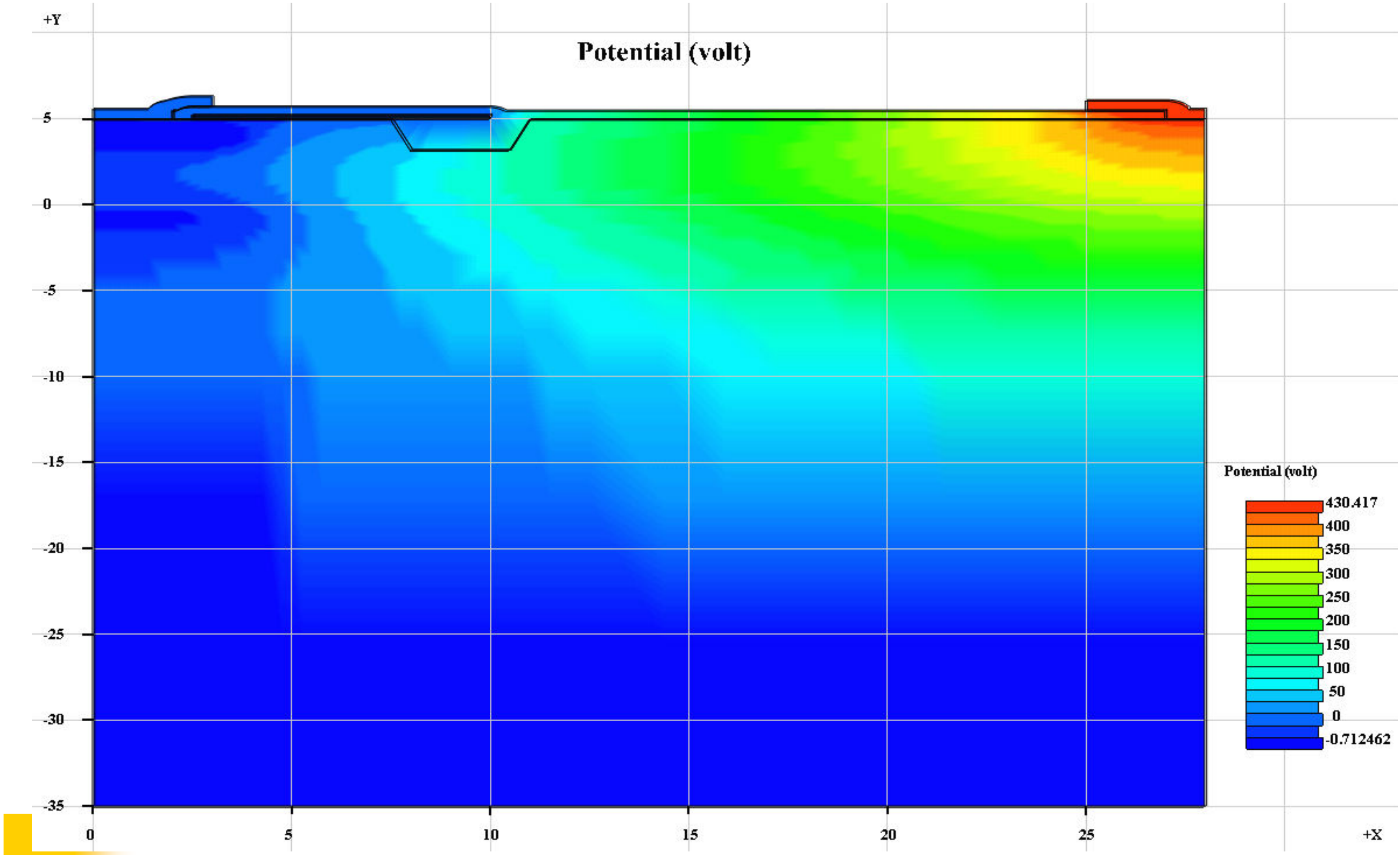
N-epi 4.0e15 cm^{-3} – Net Doping



Cut line 1

Cut line 2

N-epi 4.0e15 cm^{-3} – Potential



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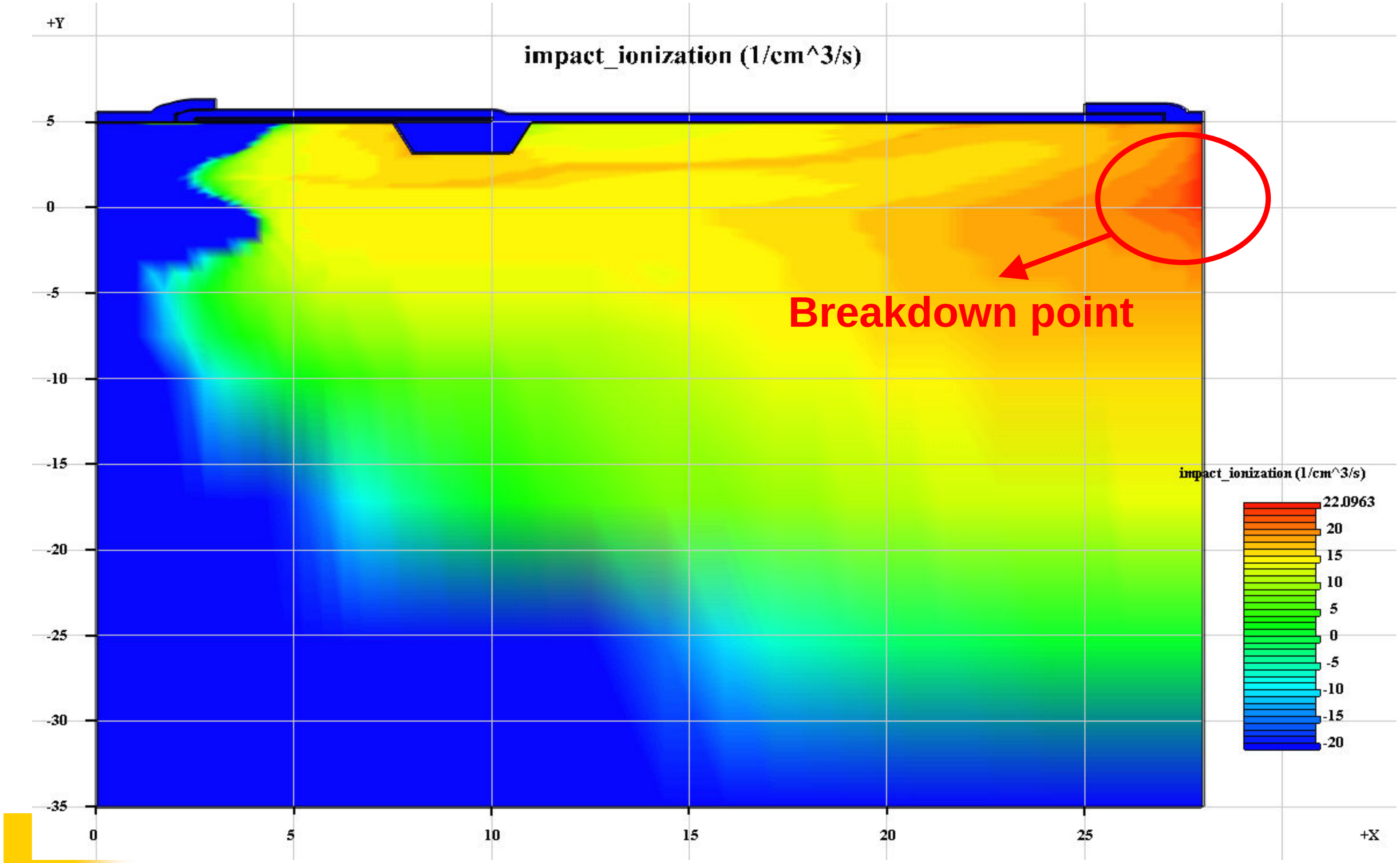
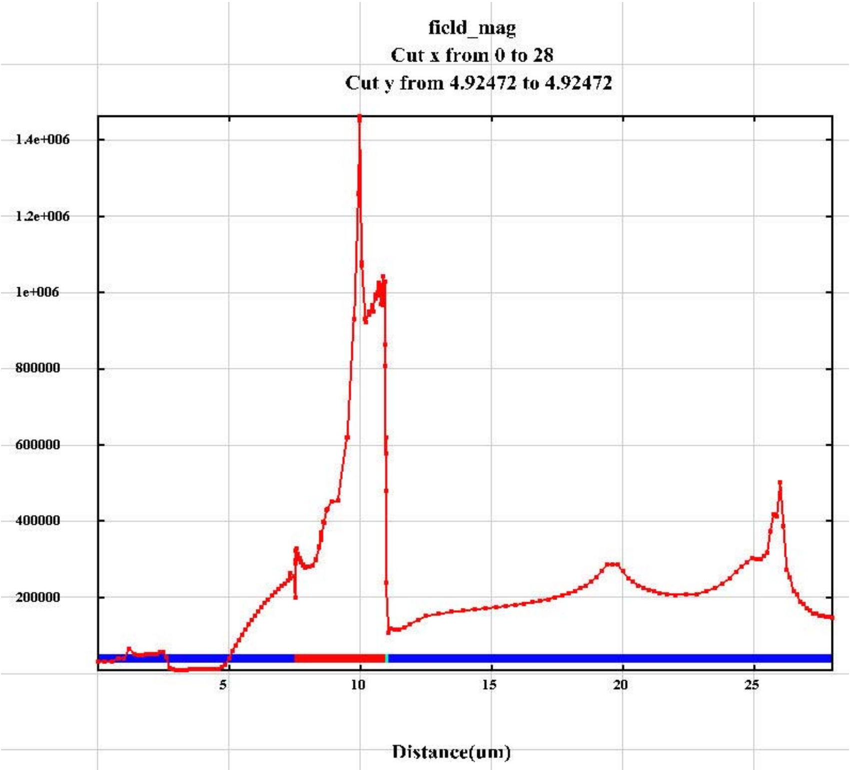
N-epi 4.0e15 cm^{-3} – Impact Ionization



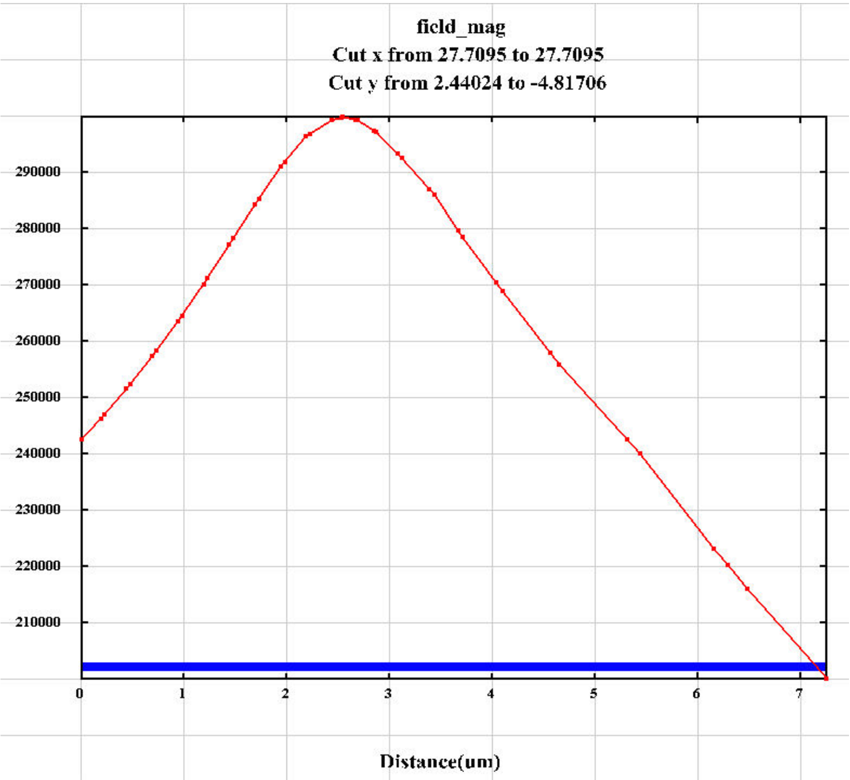
Breakdown point

N-epi 4.0e15 cm^{-3} – Electric Field

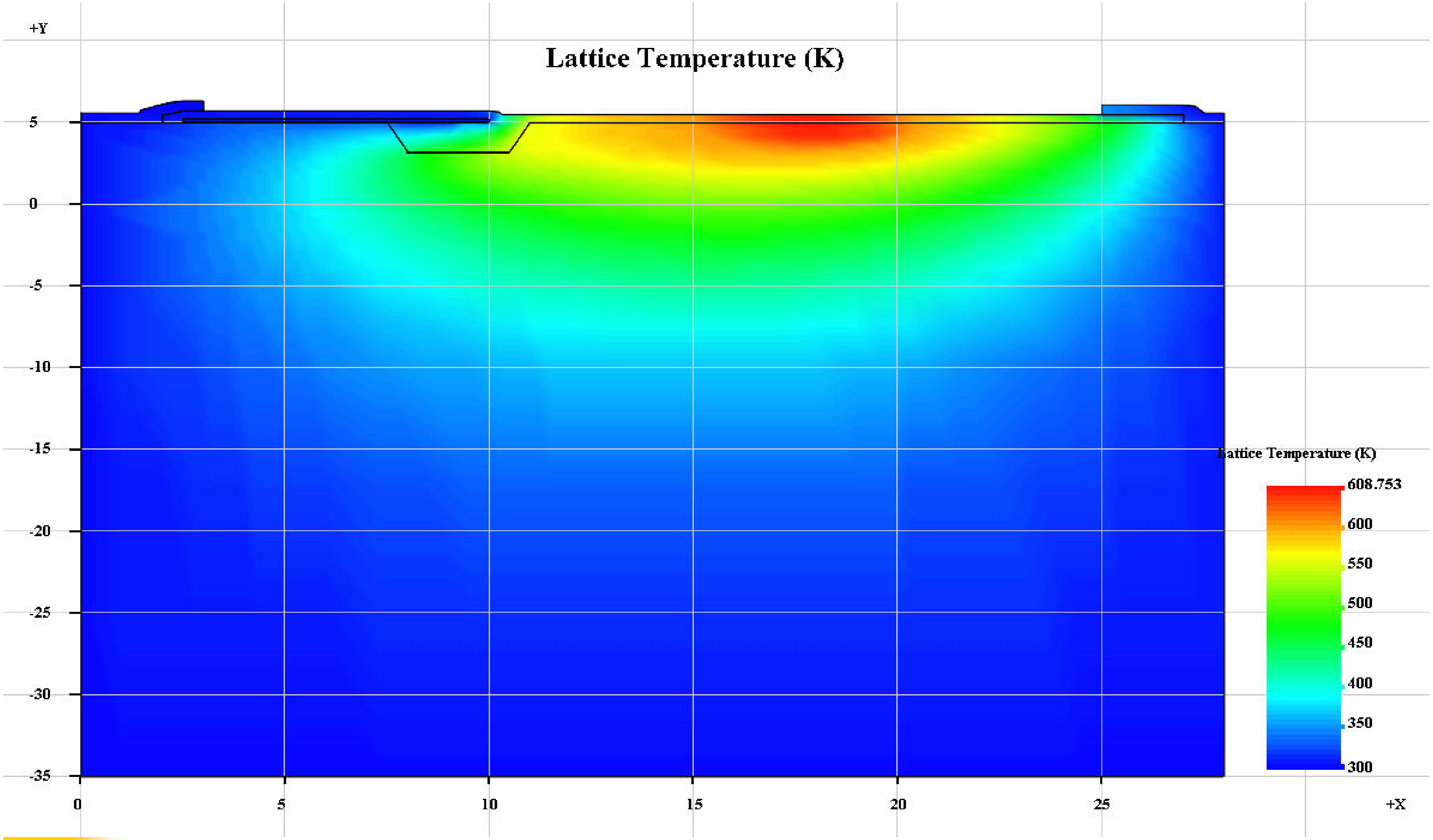
Cut line 1



Cut line 2

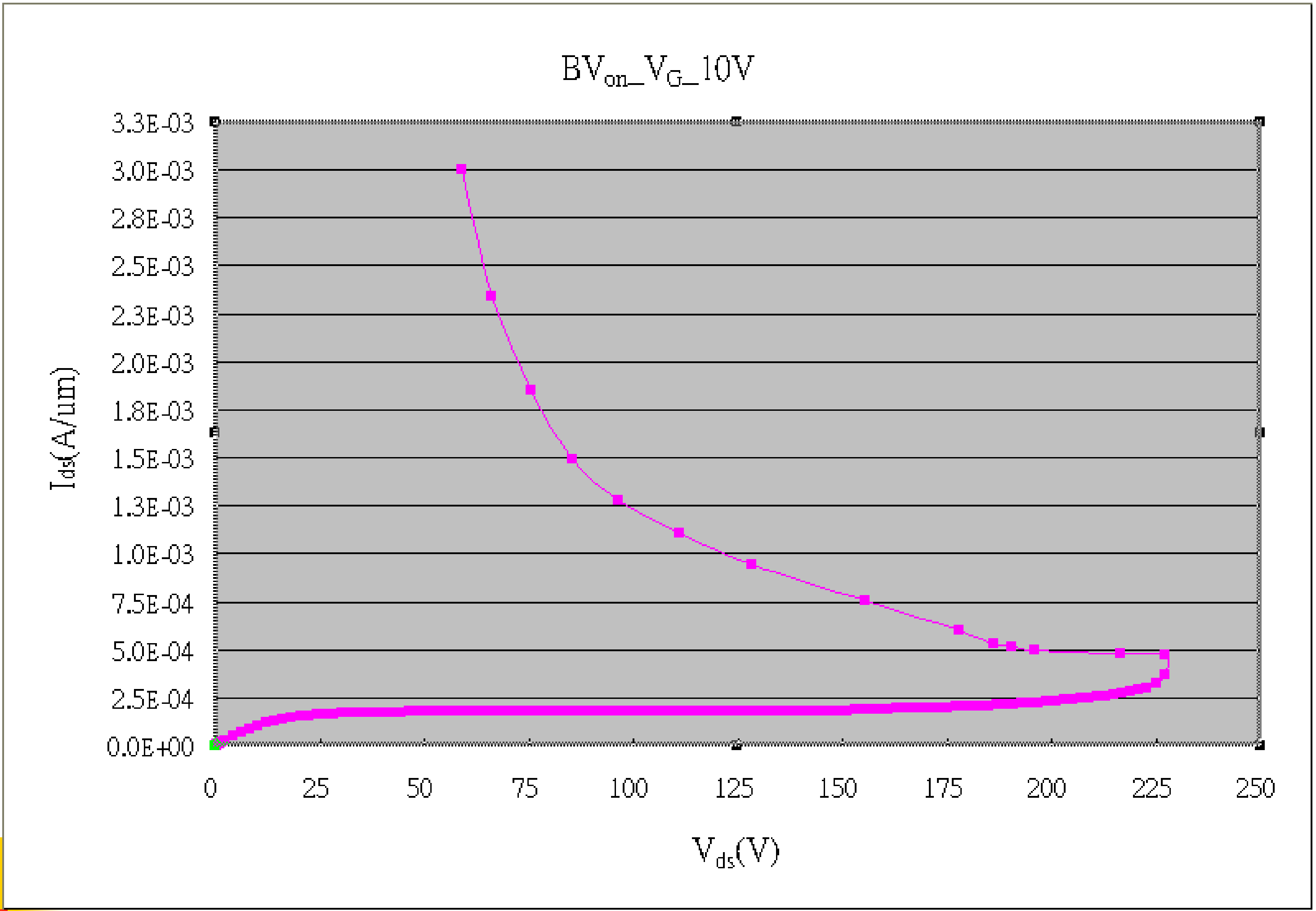


Lattice temperature (on-state)



Remark: on-state temperature distribution sensitive to thermal boundary (heat-sink, cooling thermal conductor, radiative boundary, etc.)

BV_{on}



Remark: on-state BV sensitive to self-heating conditions.

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Trend Summary

N-epi doping (1/cm^3)	BV_{off} (V)	R_{dson} (m$\Omega \cdot$ cm^2)	BV_{off} / R_{dson} (V / m$\Omega \cdot$ cm^2)	Breakdown Point
4.0e15	430.4	23.4	18.38	Drain verical
4.7e15	438.6	20.7	21.14	Drain verical
5.5e15	326.7	18.50	17.66	Gate

Remark: Crosslight gets reasonable trend of breakdown position.

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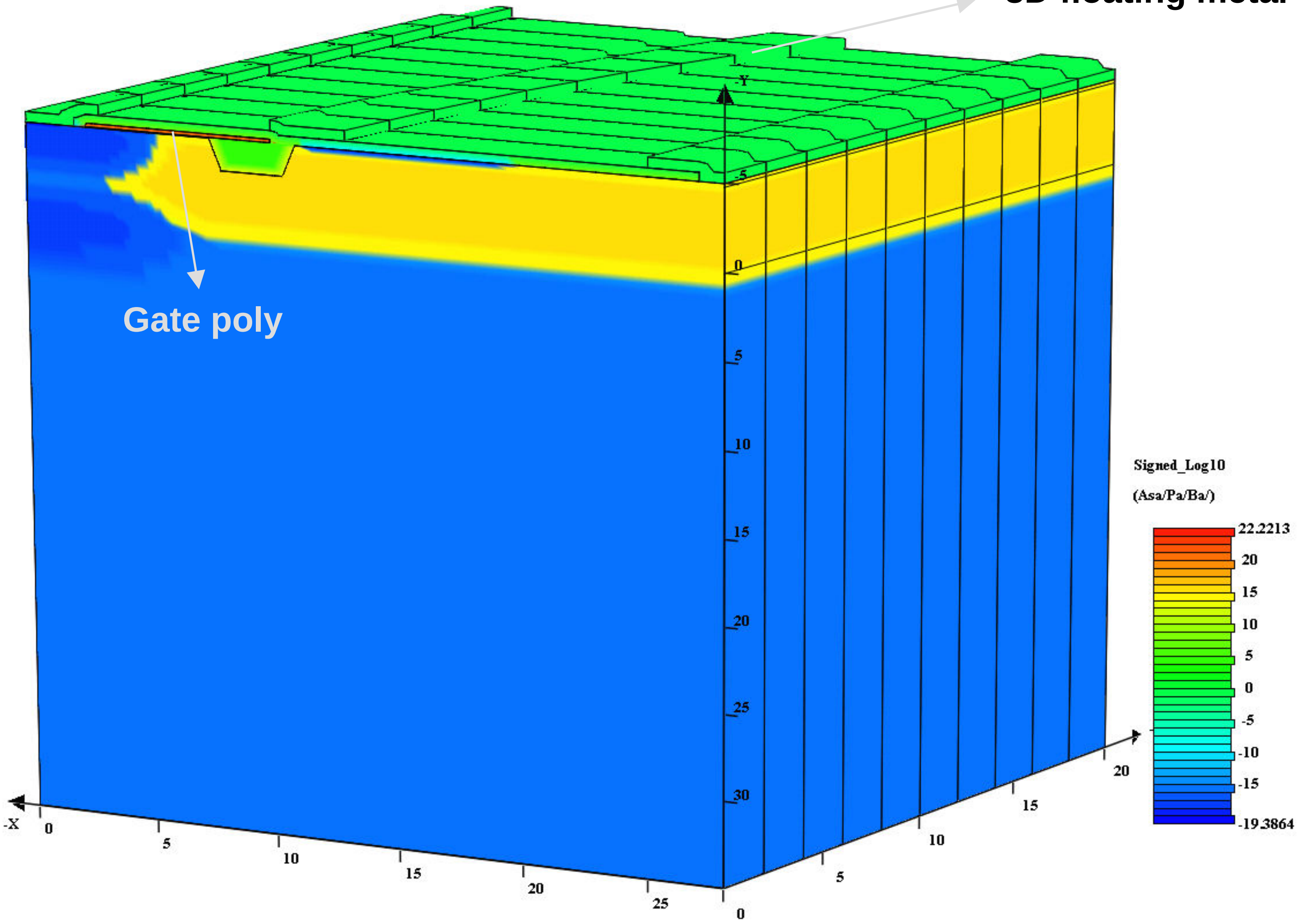
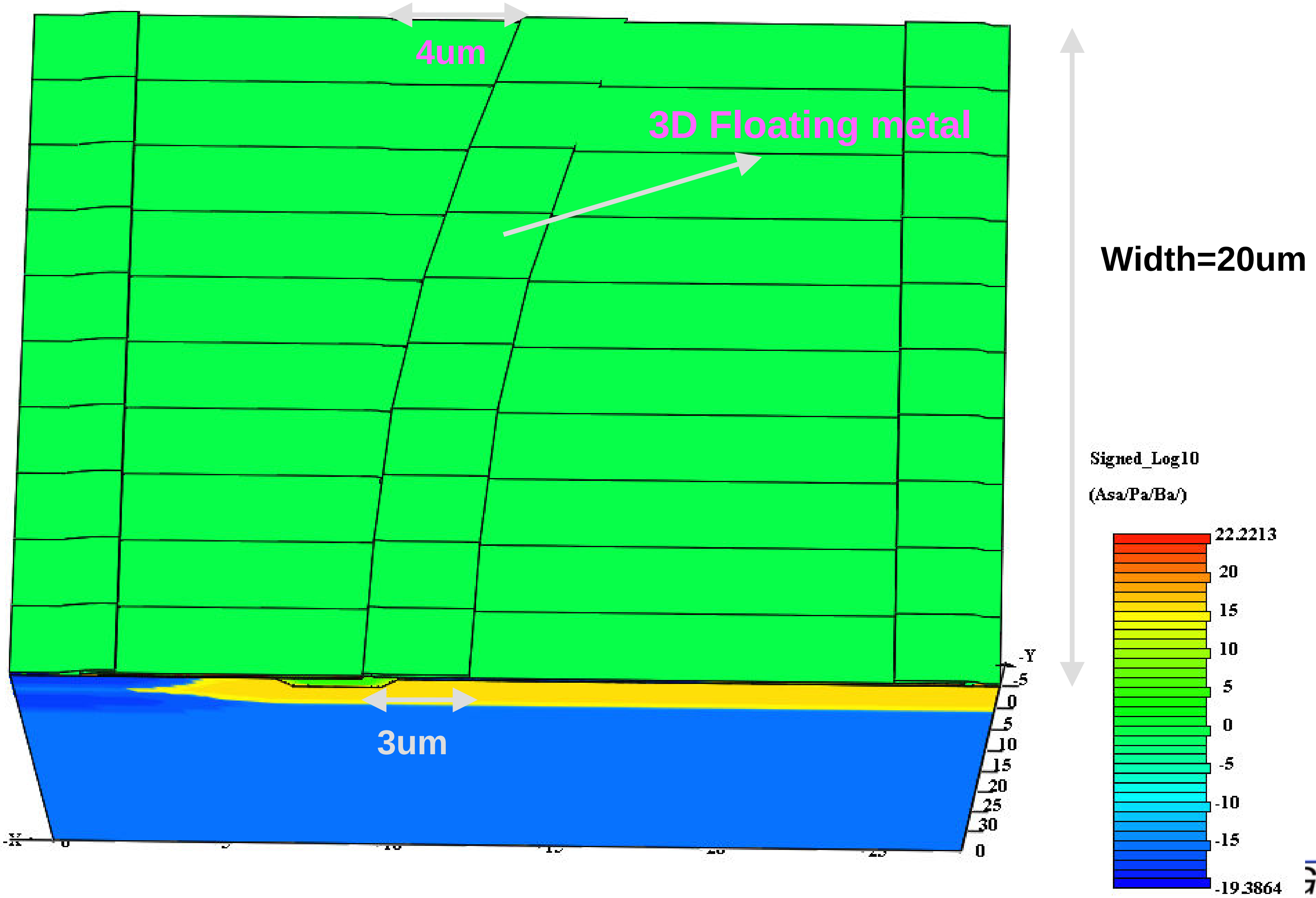
3D floating metal – Structure – 1



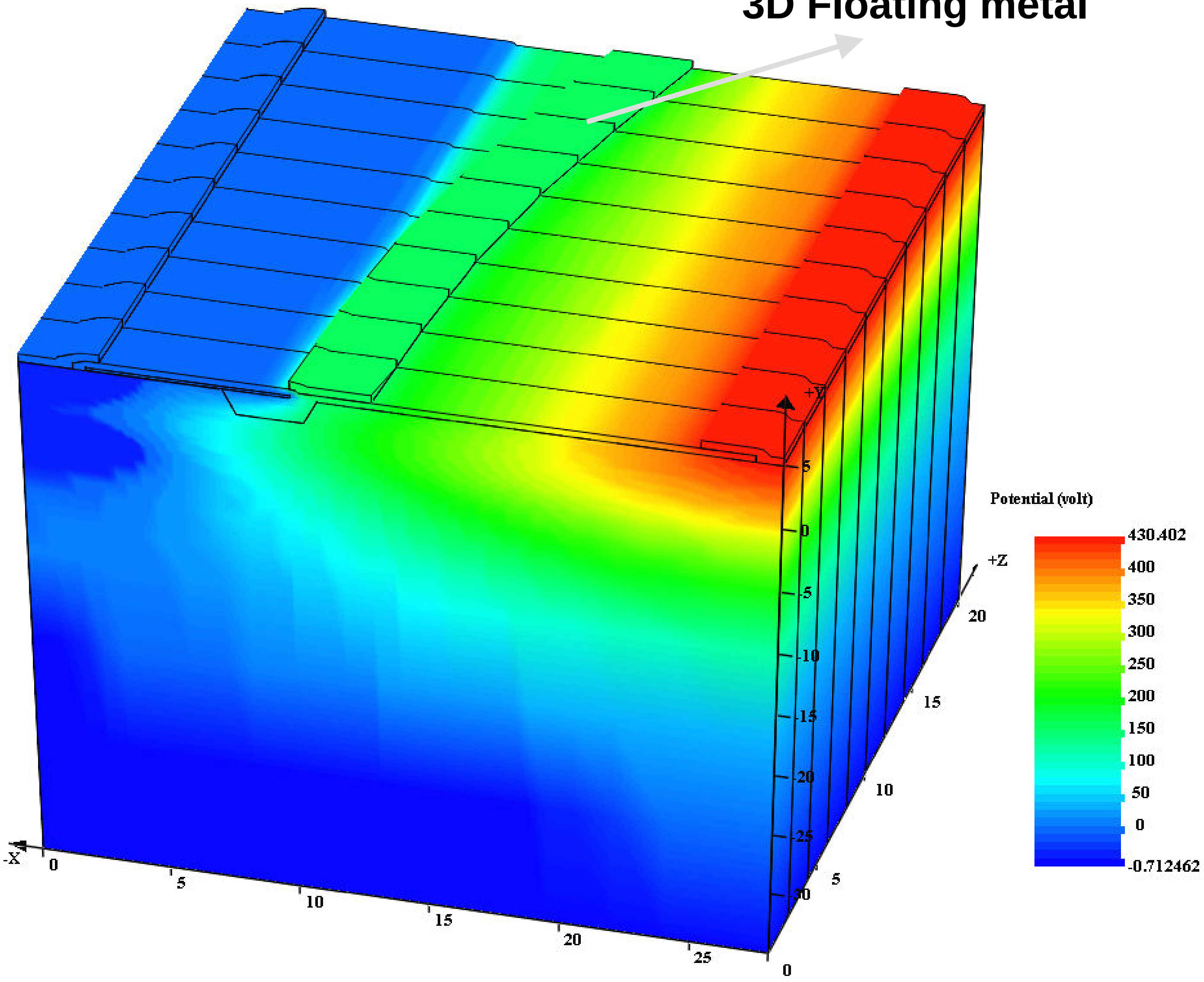
3D floating metal

Gate poly

3D floating metal – Structure – 2



3D floating metal – Potential

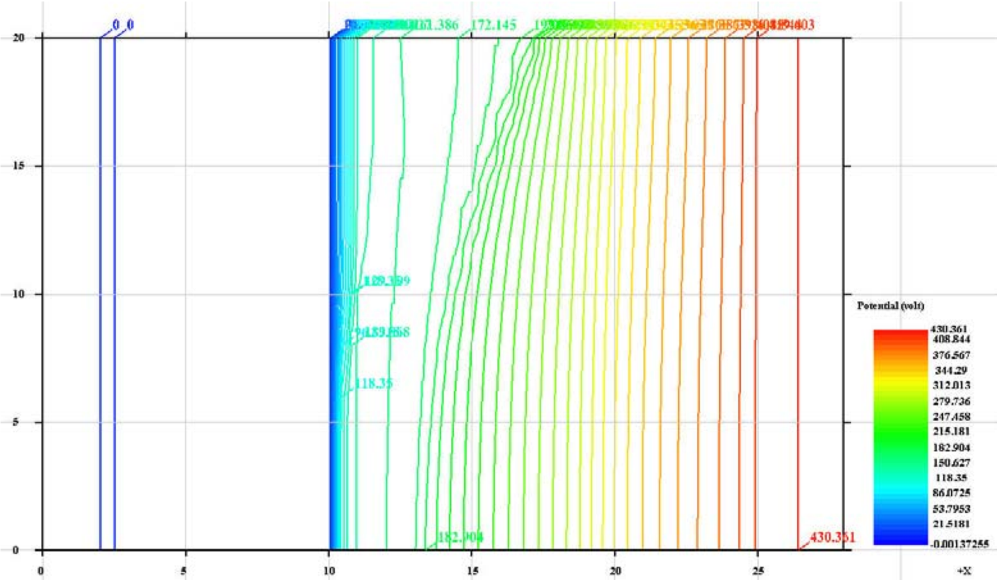


3D Floating metal

3D floating metal – Potential

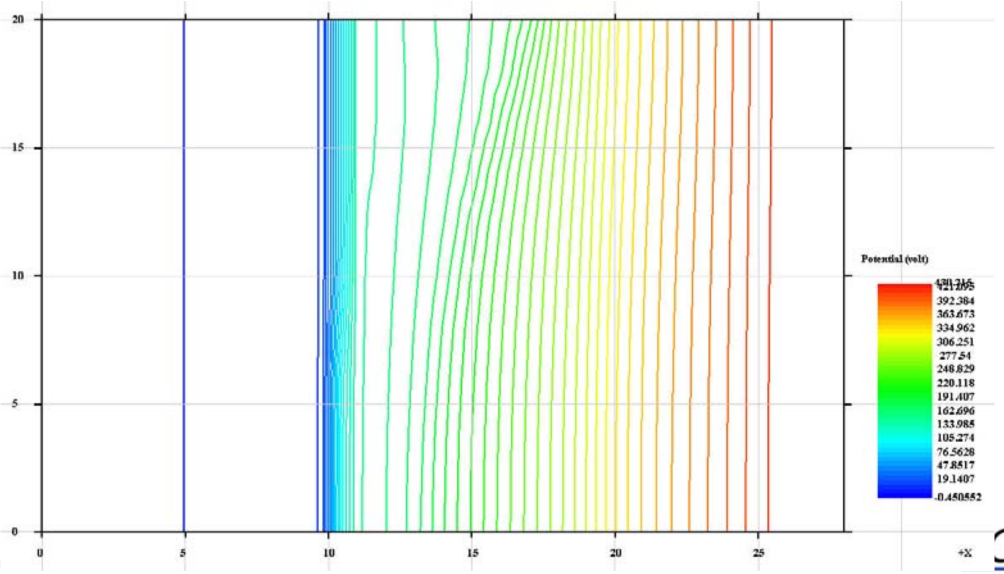
XZ plane :

The same height as gate poly

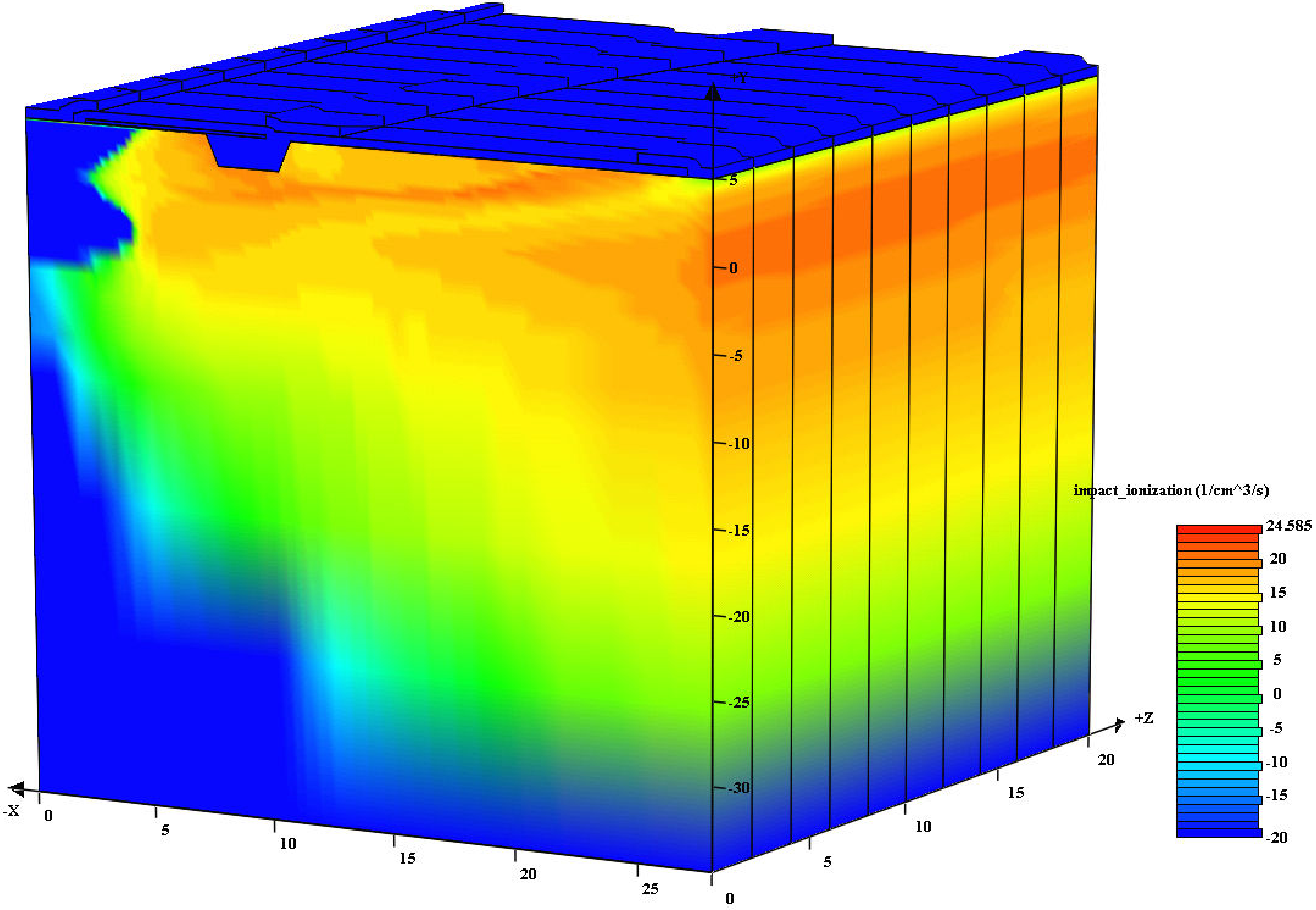


XZ plane :

Silicon surface



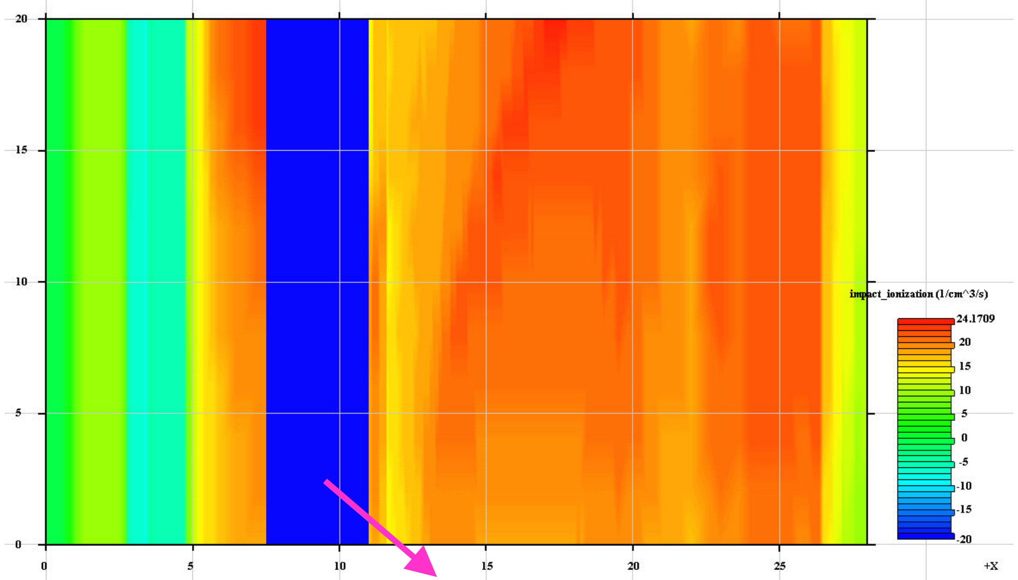
3D floating metal – Impact ionization



3D floating metal – Impact ionization

XZ plane :

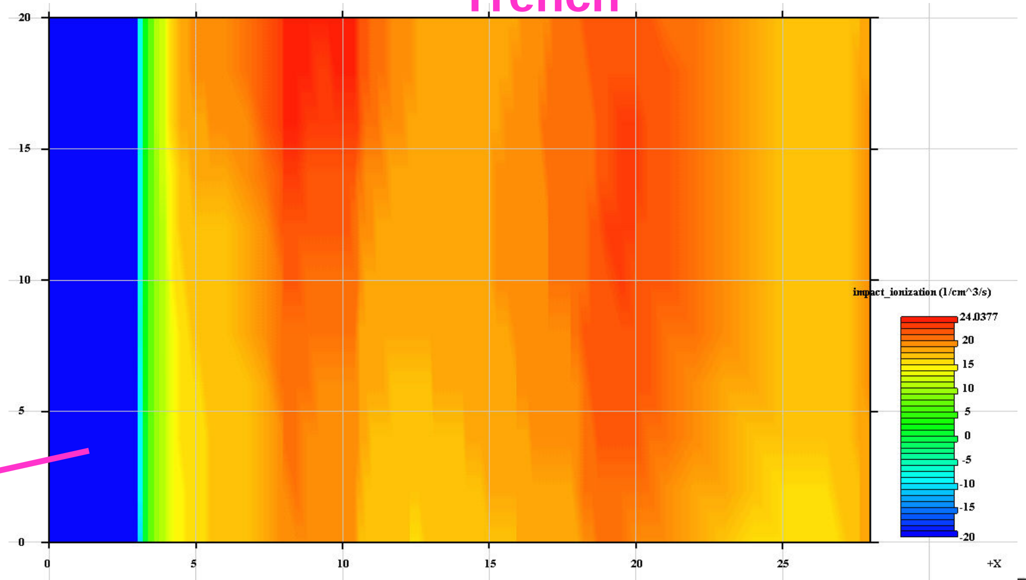
Silicon surface



Trench

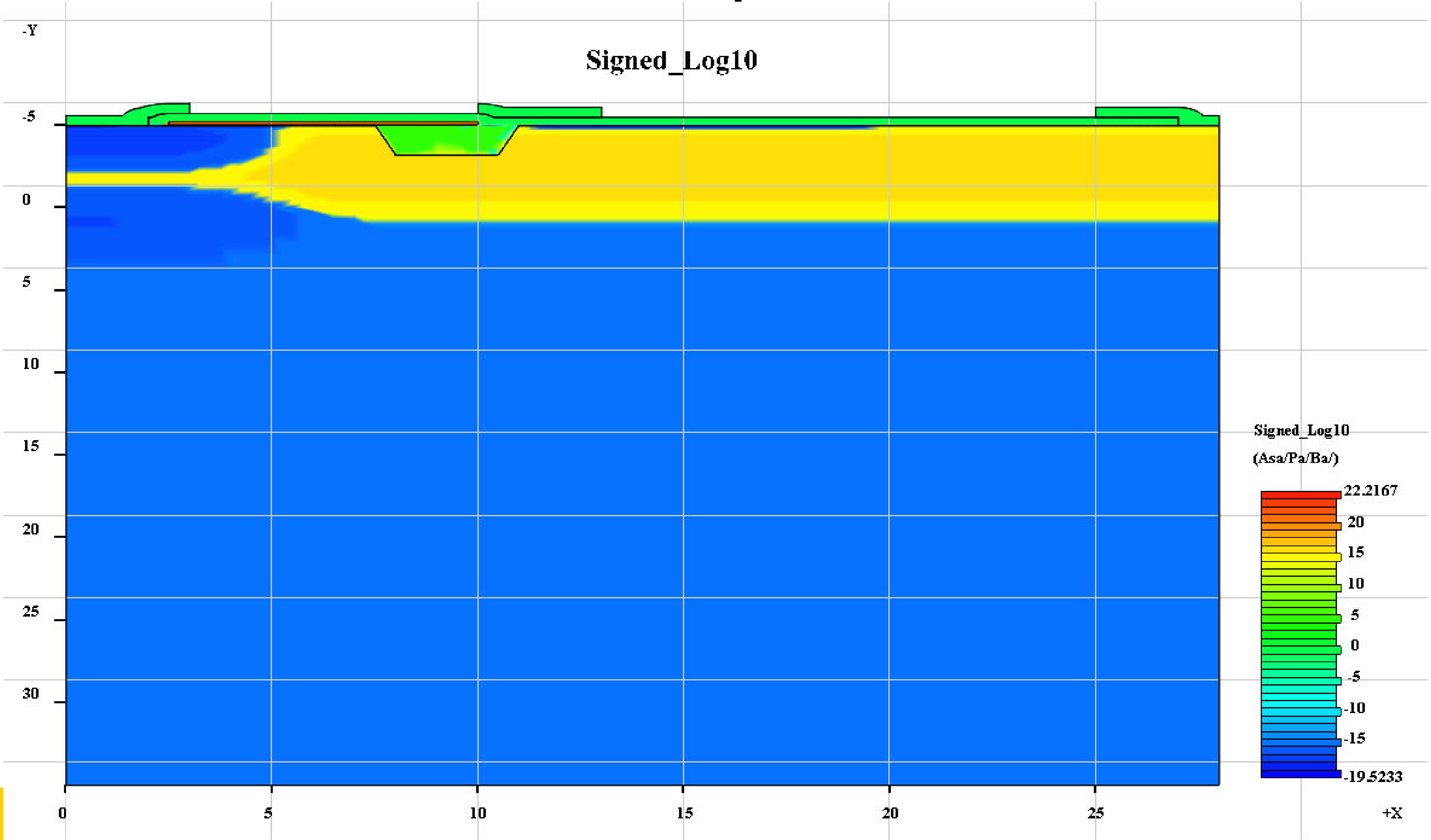
XZ plane :

Trench bottom

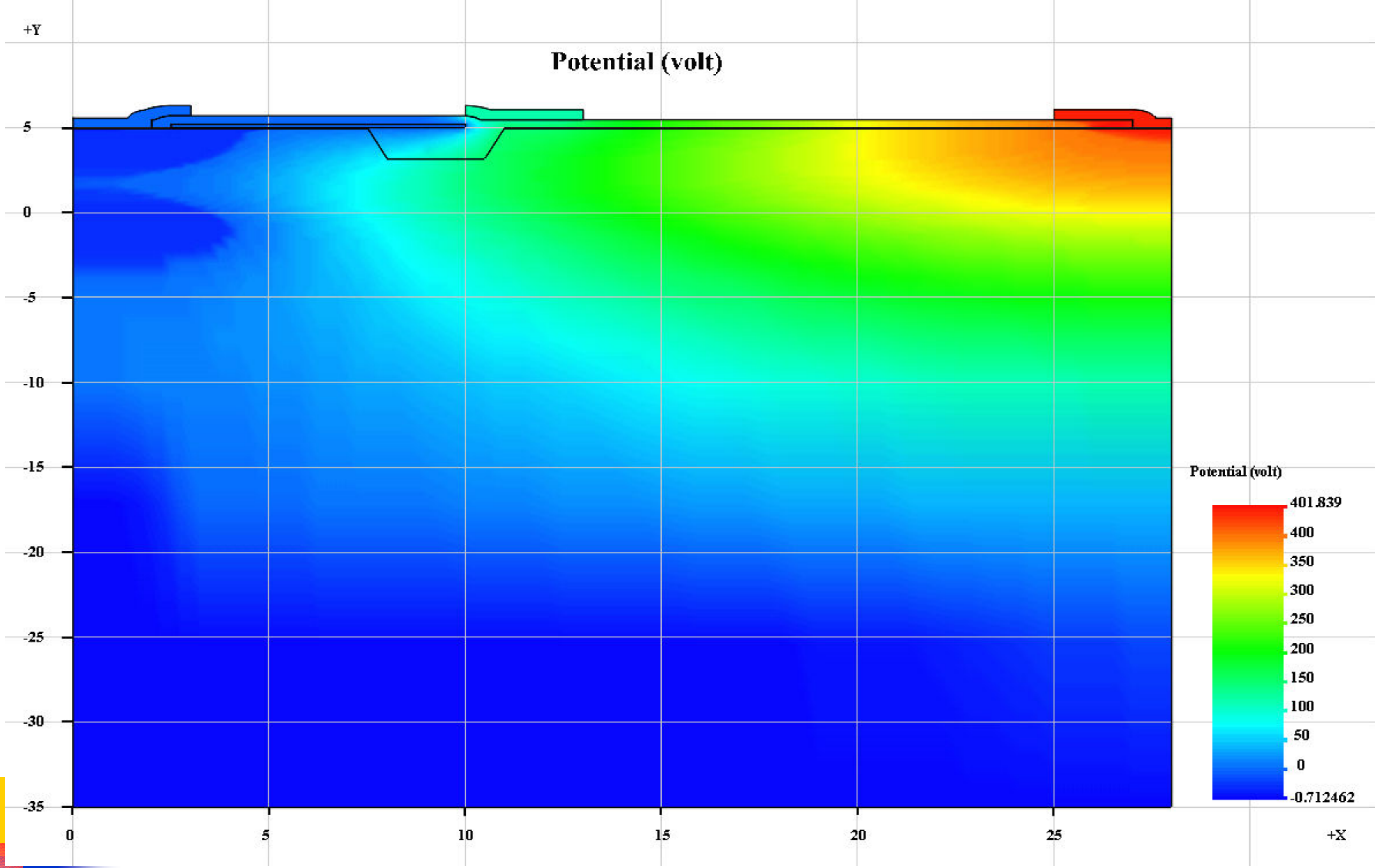


P-body region

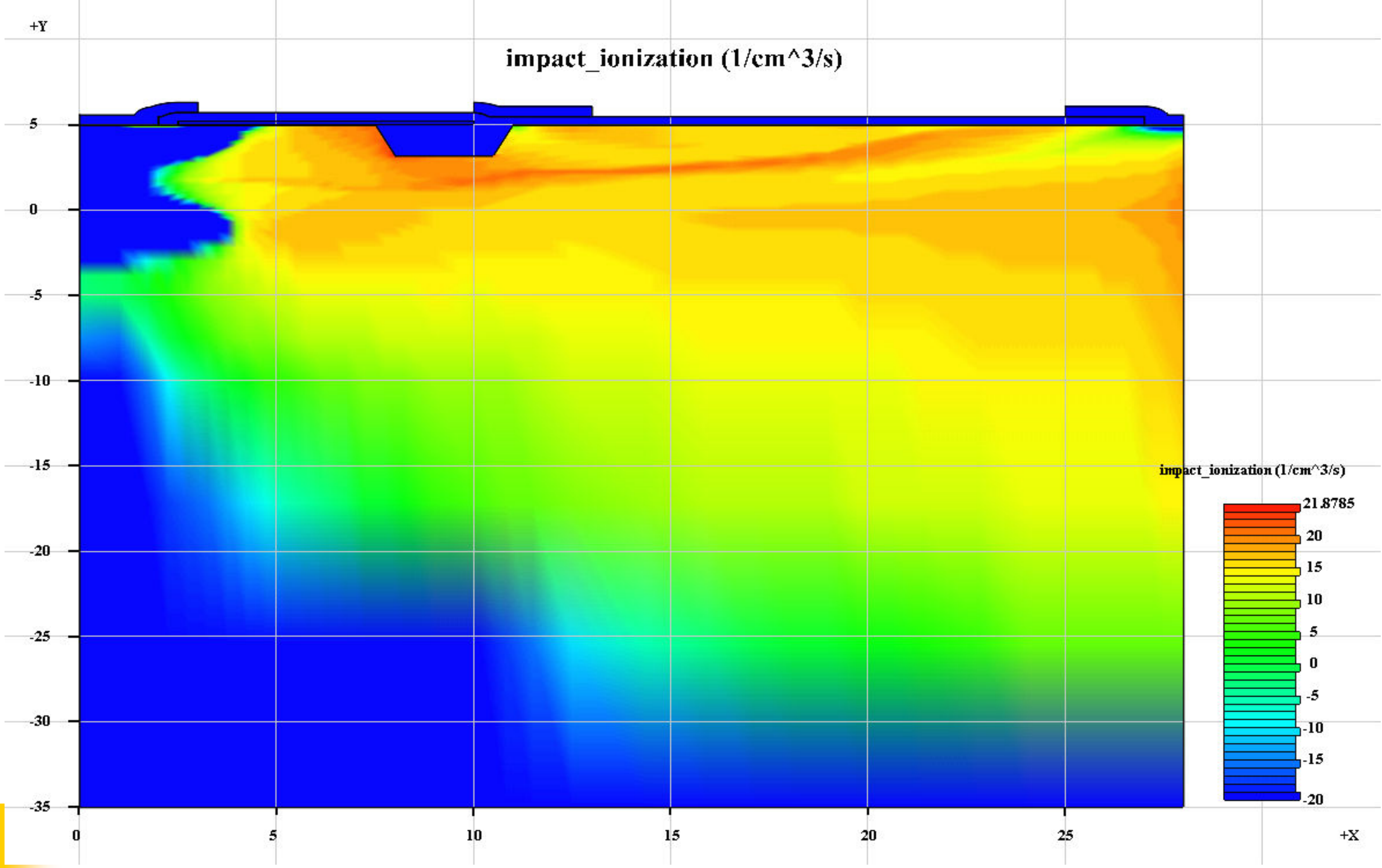
2D case – Z=0 plane – Structure



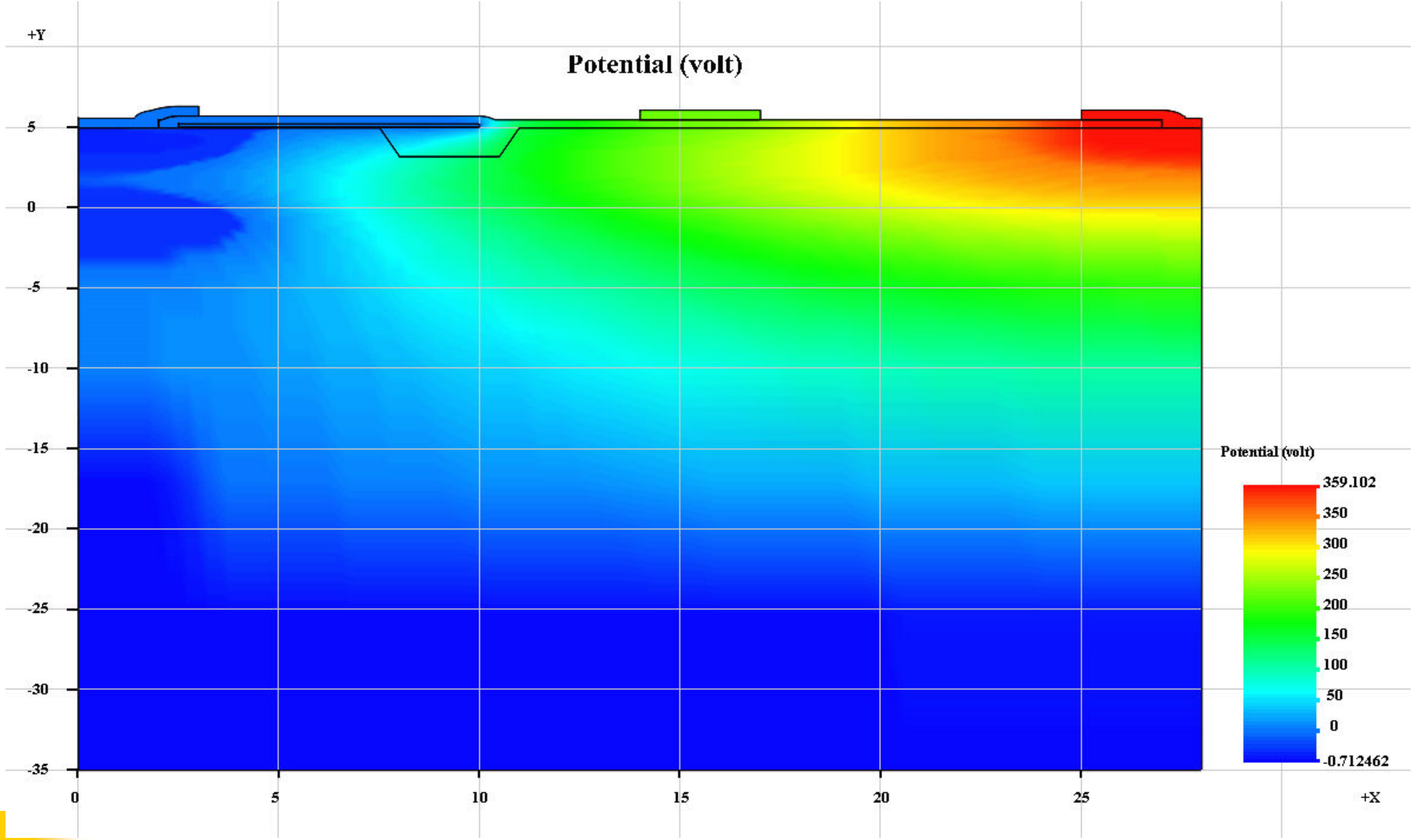
2D case – Z=0 plane – Potential



2D case – Z=0 plane – Impact ionization



2D case – Z=20 plane – Potential



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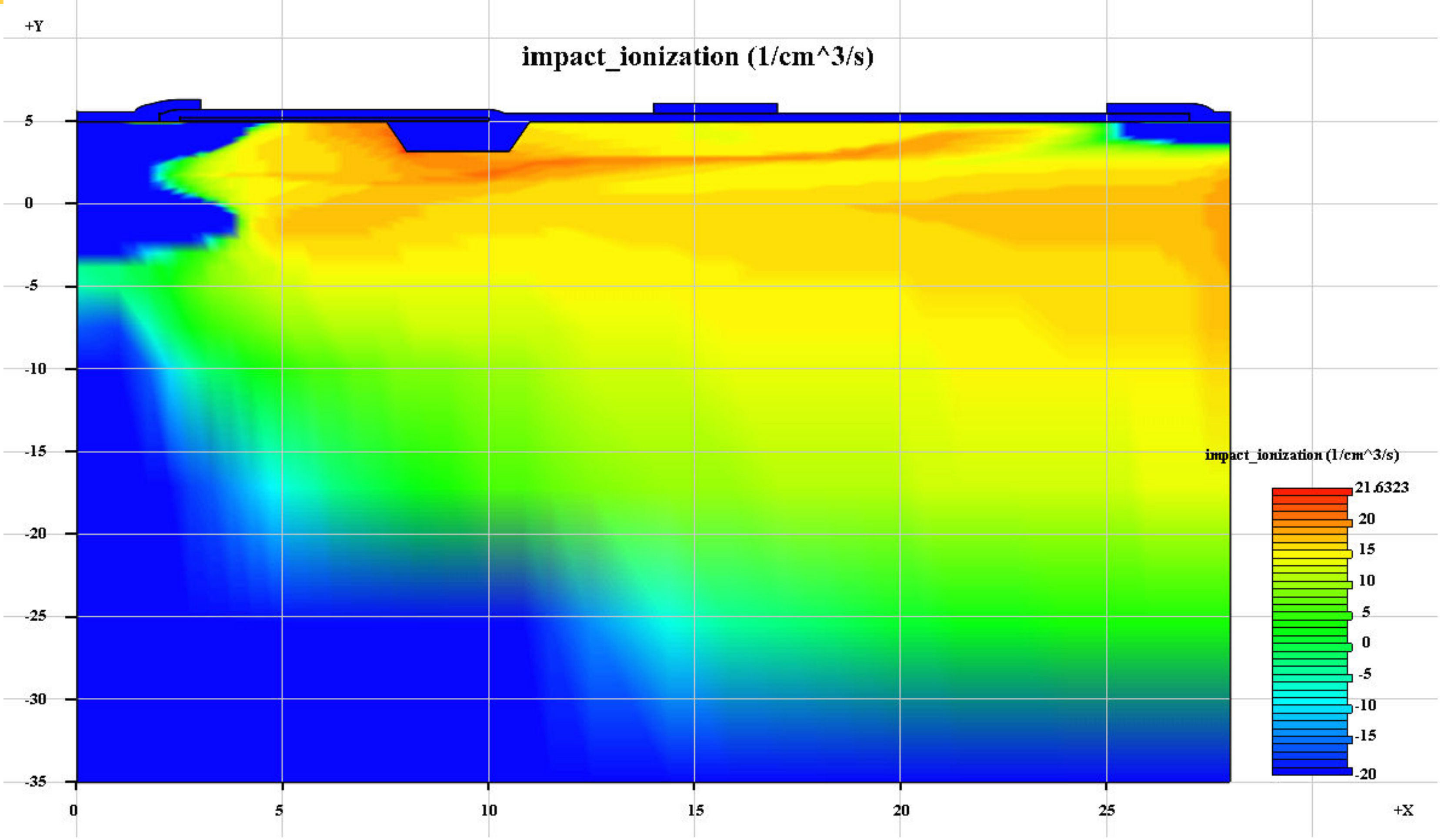
2D case – Z=20 plane – Impact ionization



Remark: FM seems to push II region away from Si surface and thus alter BVoff

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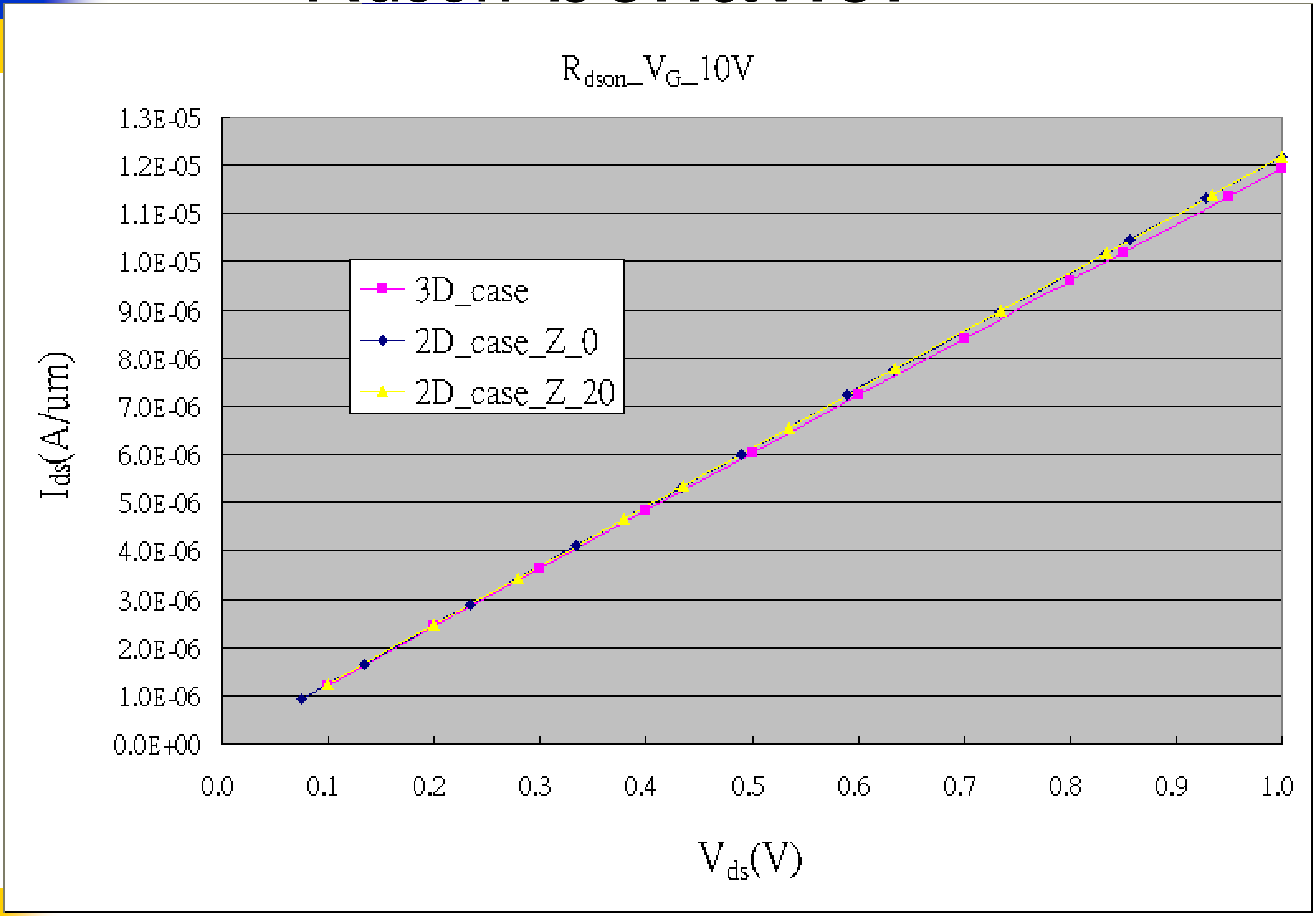
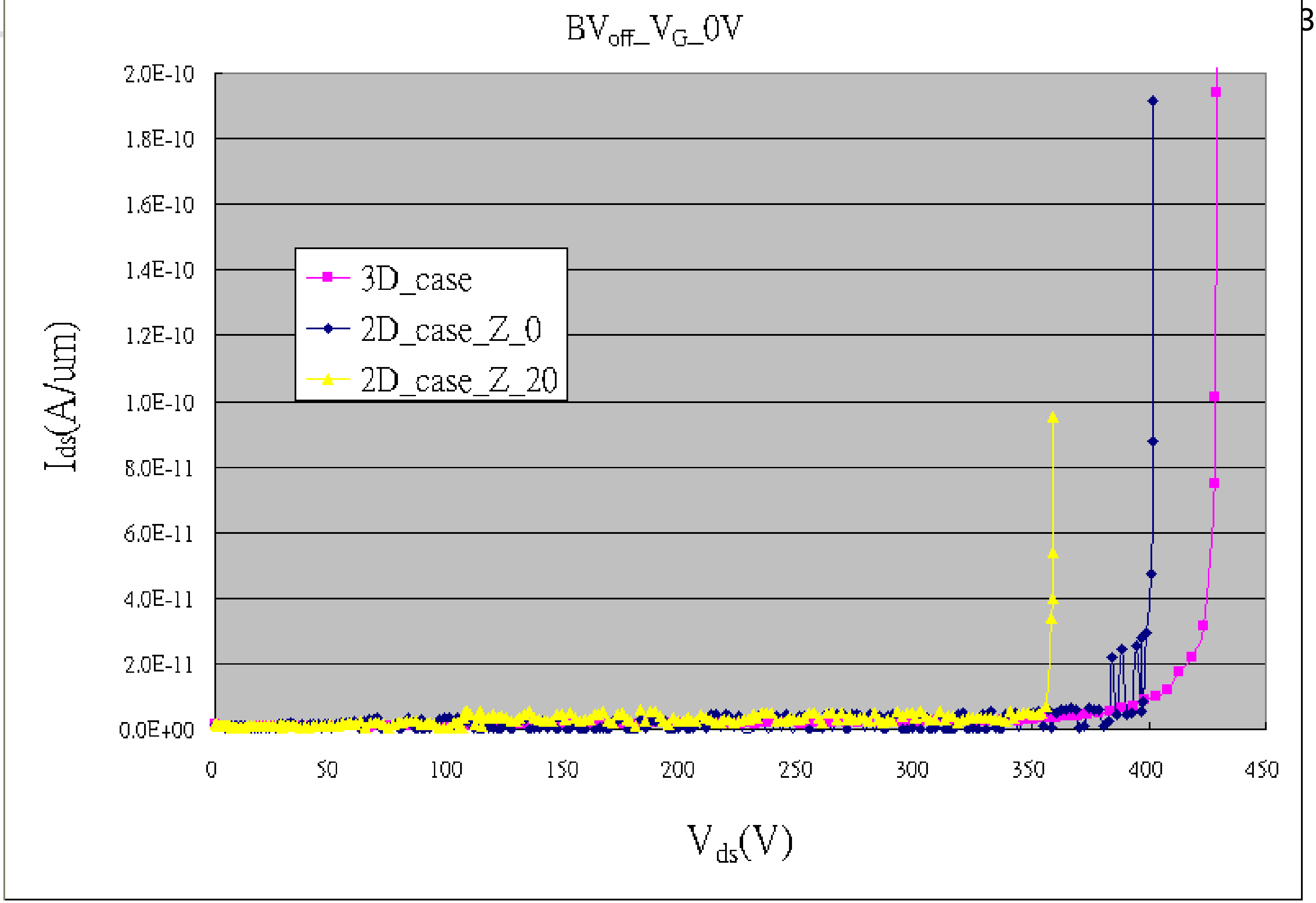
Rdson behavior



FM does not alter Rdson

BV_{off}



Remark: For 2D, FM near poly gate pushes II region away from trench corners and seems to delay breakdown; 3D: angled FM appears to perform better.

3D Summary

	BV (V)	R_{dson} (mΩ · cm^2)	BV / R_{dson} (V / mΩ · cm^2)
2D_case_Z_0	402	19.30	20.83
2D_case_Z_20	359	19.30	18.20
3D_case	430	19.69	21.84

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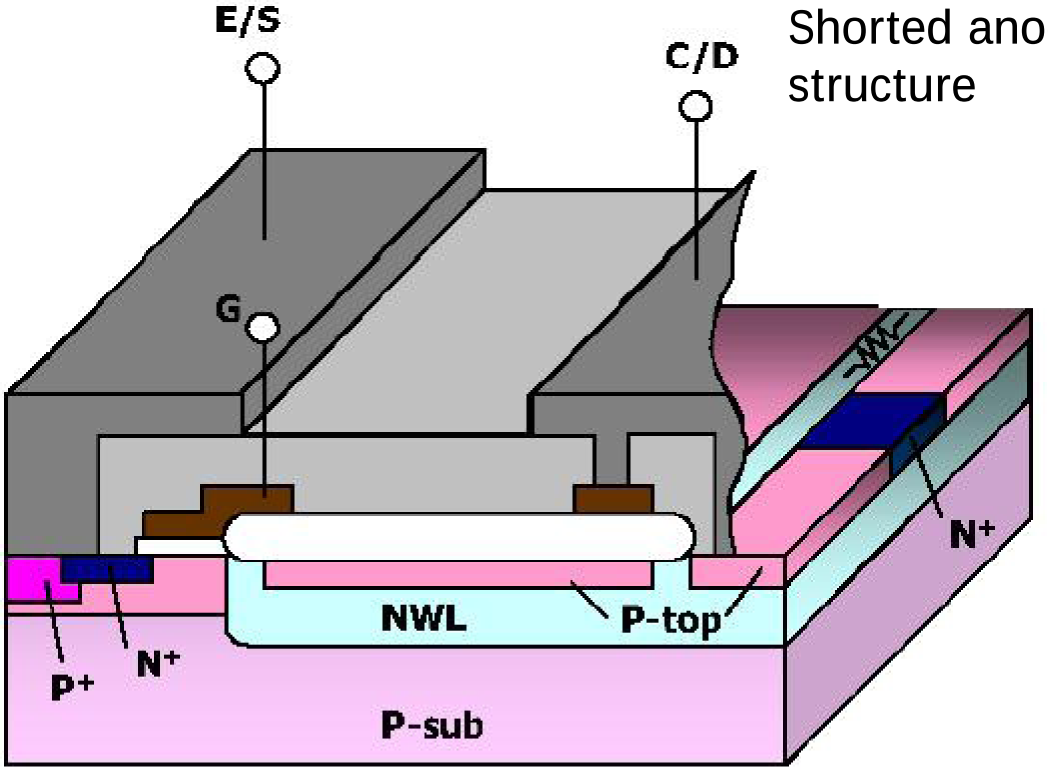
A new hybrid IGBT

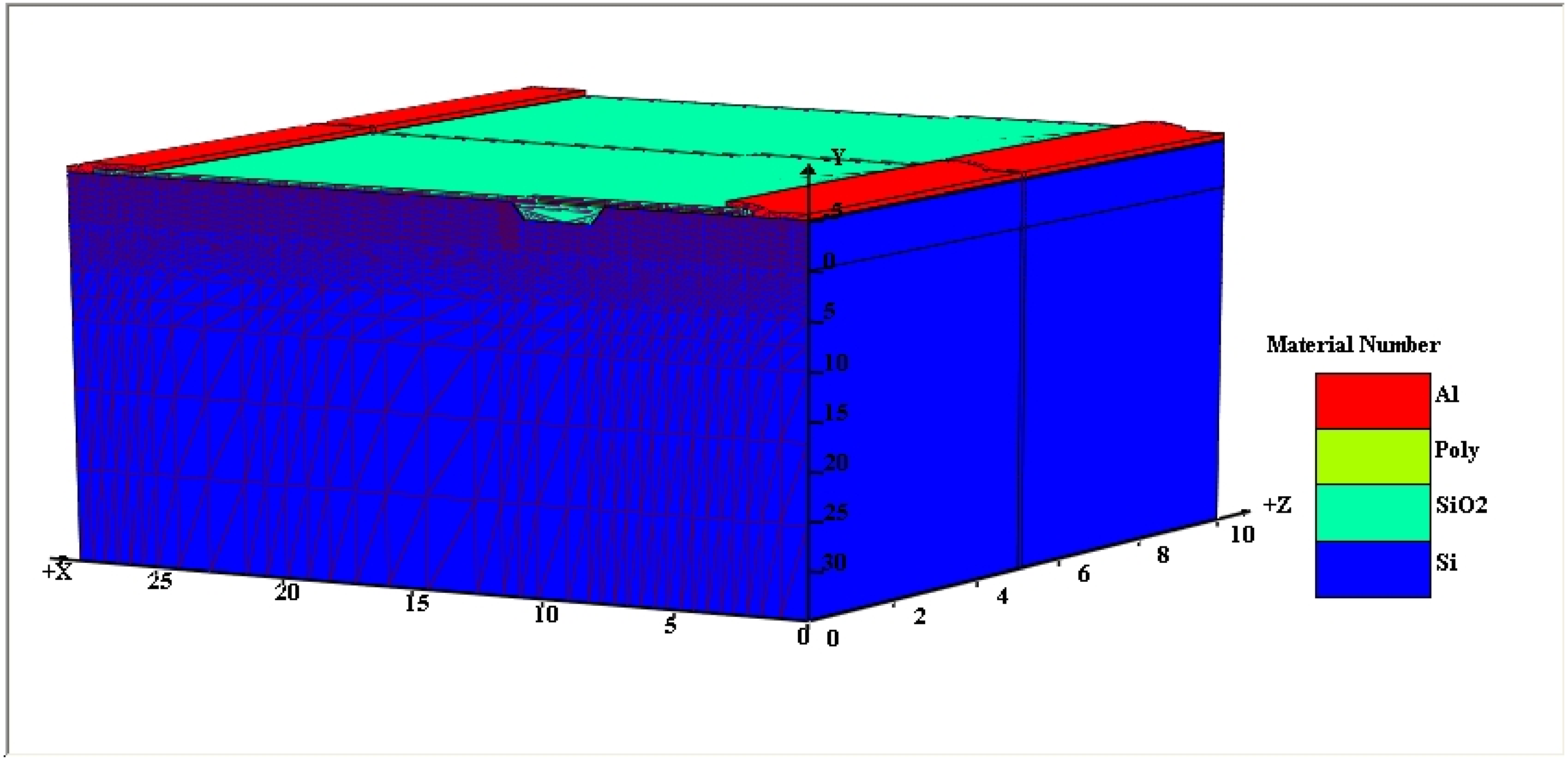


Shorted anode structure

Remark: May be regarded as LIGBT+LDMOS in 3D

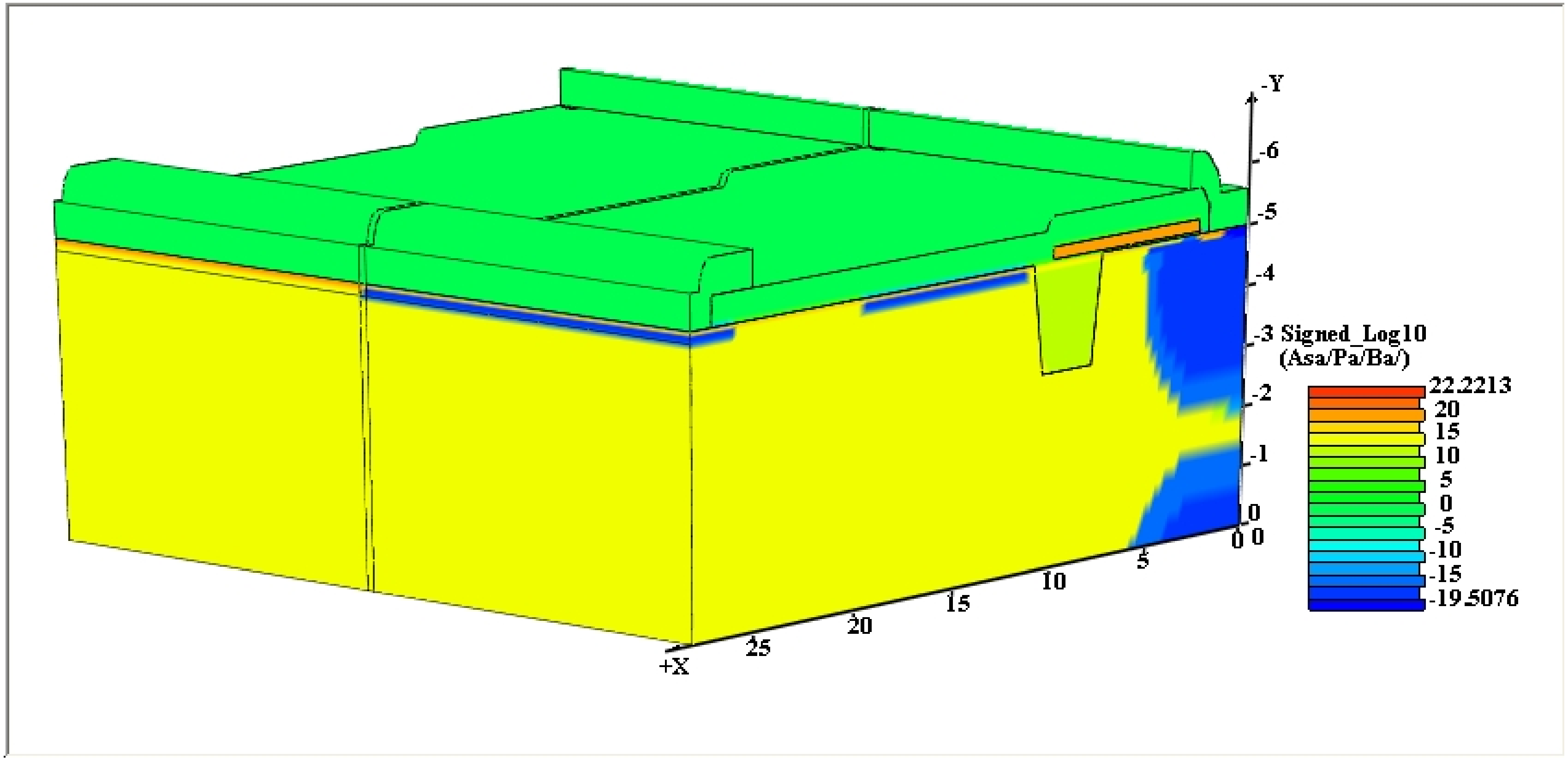
Ref: S. Kaneko, et.al., Proc. 19th Int. Symp. Power Semicon. Devices & Ics, 2007,p. 17

A quick 4-plane 3D demo



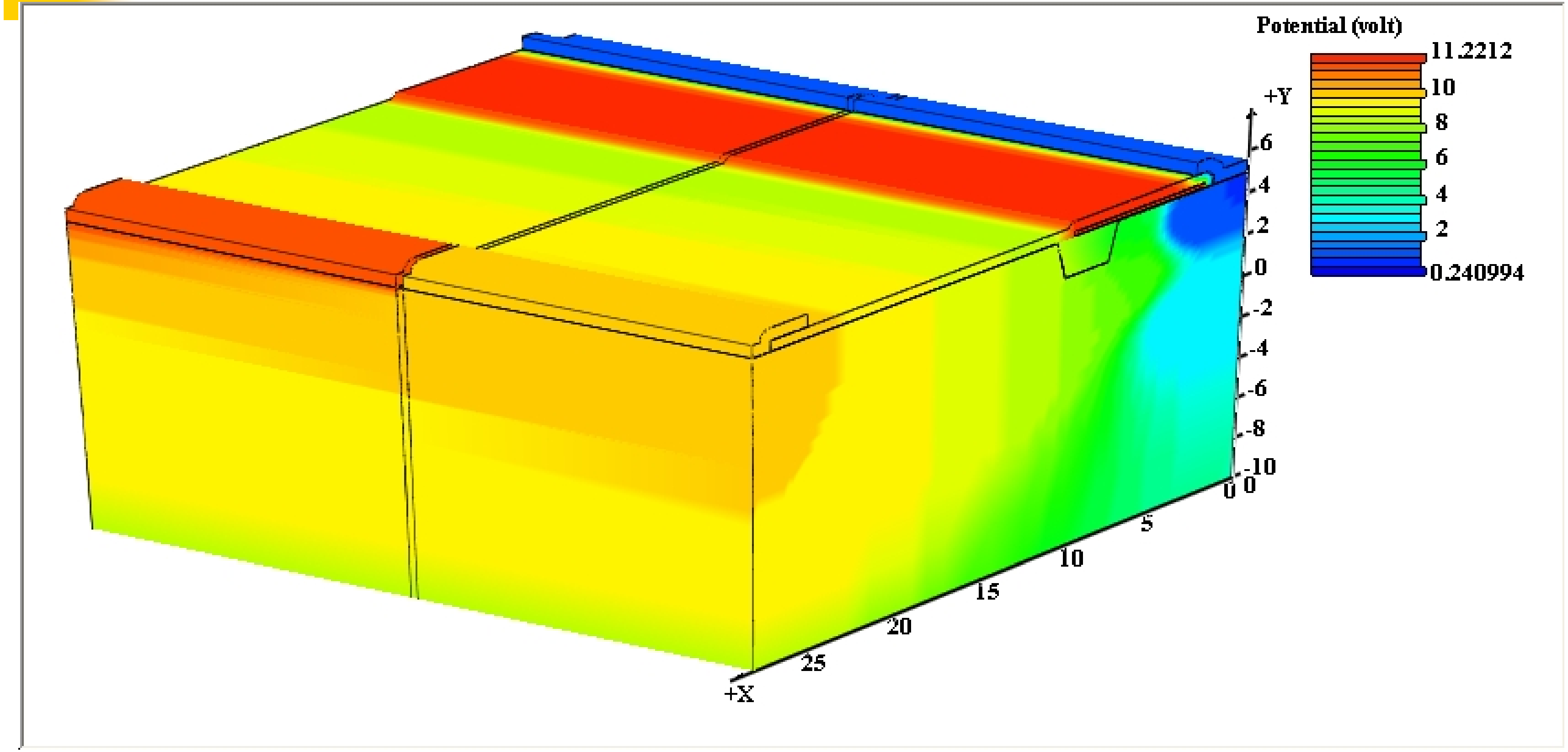
Process simulation: combined quasi-3D and full-3D modes. Device simulation: full-3D mode.

3D net doping



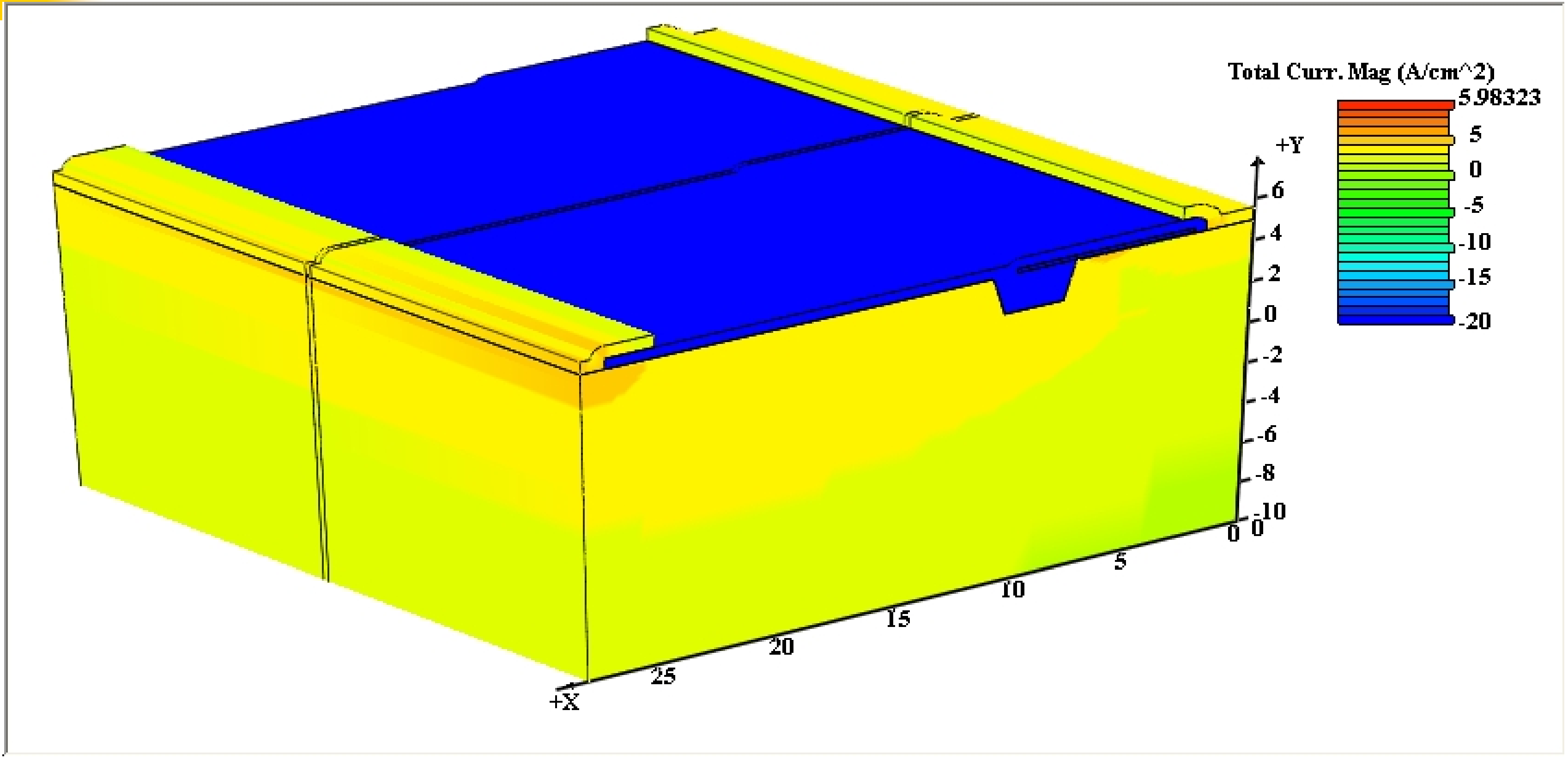
Process simulation: combined quasi-3D and full-3D modes. Device simulation: full-3D mode.

3D potential



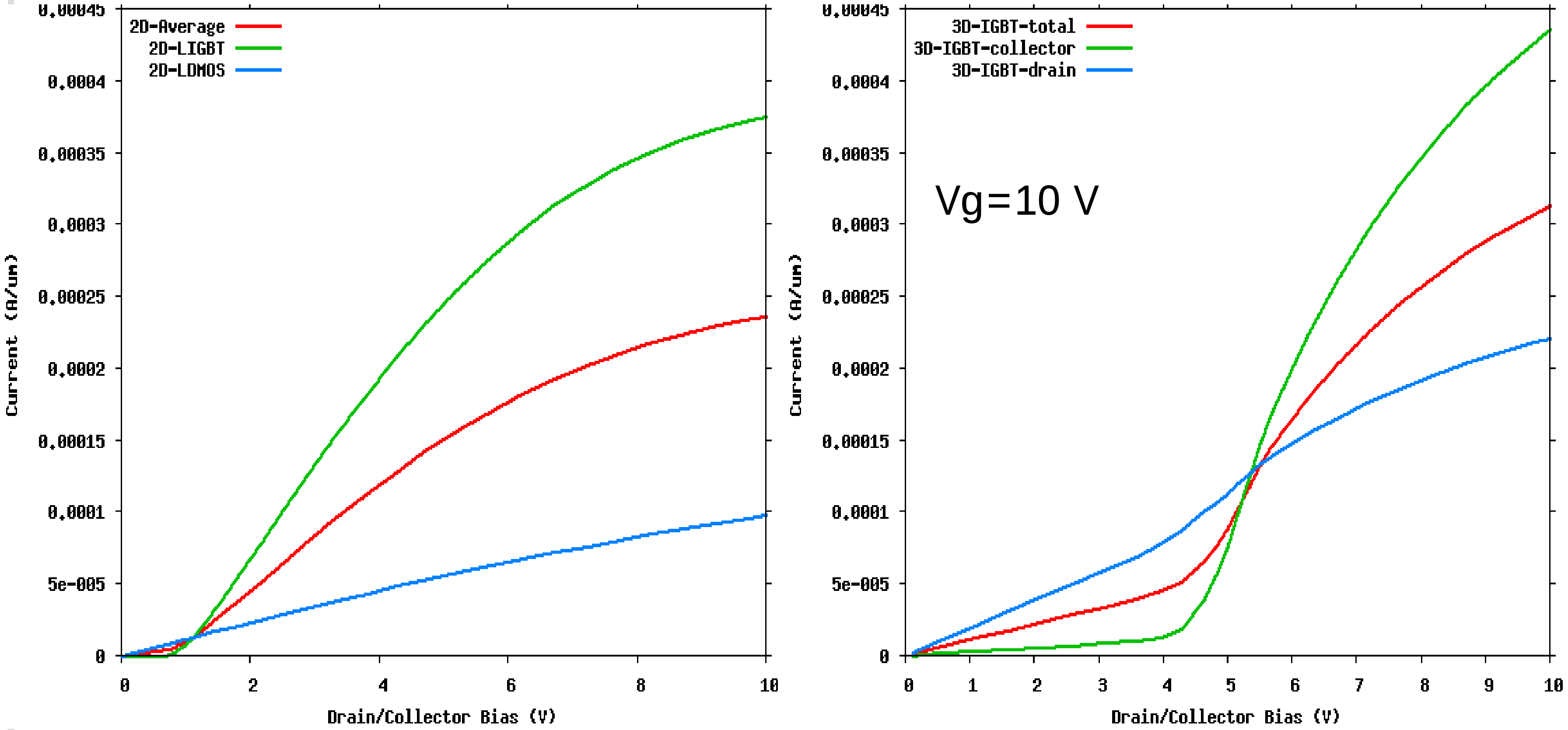
LIGBT collector metal work function adjusted to provide low-barrier ohmic contact to p-top region. At Vg=10 V, Vd=Vc=10 V.

3D current magnitude (log10)



At Vg=10 V, Vd=Vc=10 V.

Comparison of 2D vs. 3D



➔ 3D result is NOT simple average of 2D.

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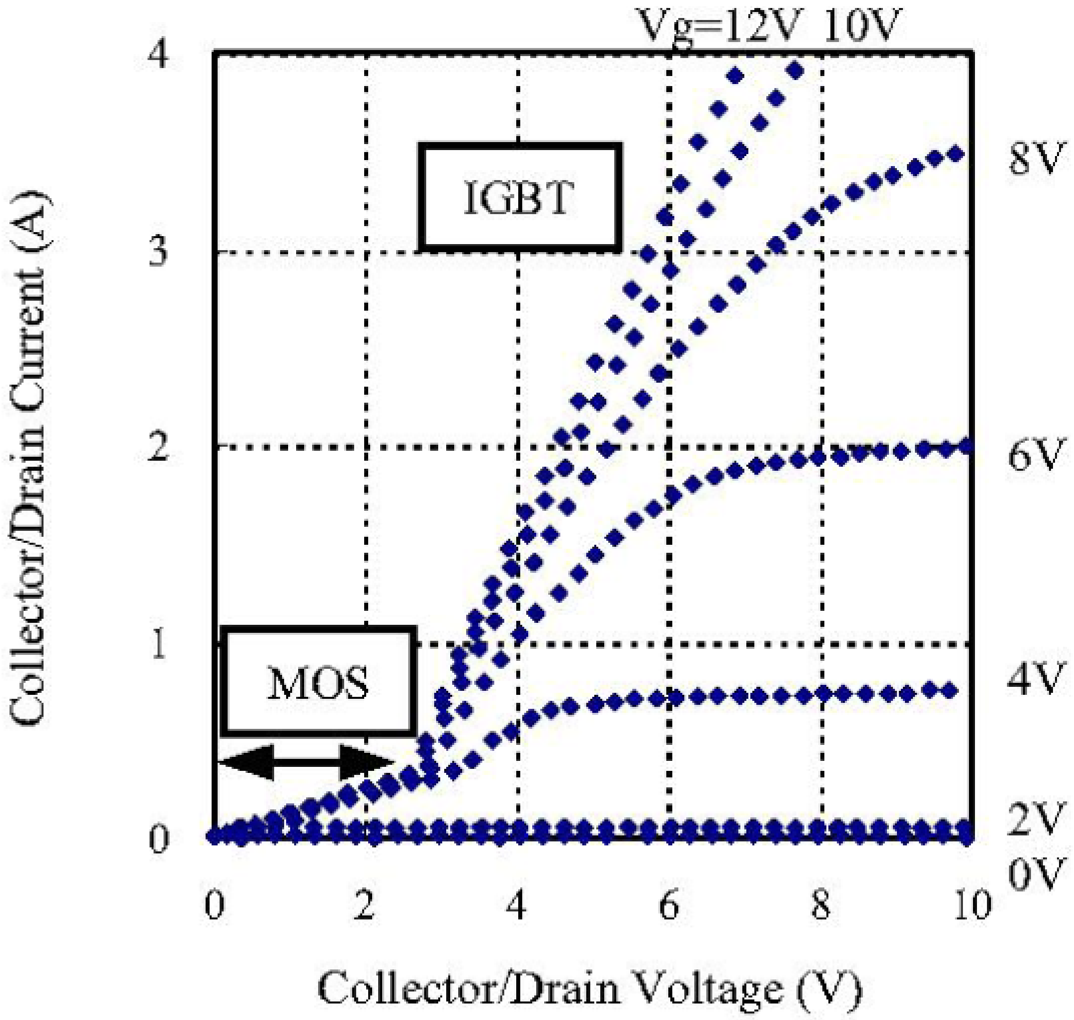
Experimental



Remark:

➔Reasonable agreement of trends achieved.

➔ 3D results agree better than simple average of 2D results.

➔ Better agreement may be achieved with more mesh planes.

Ref: S. Kaneko, et.al., Proc. 19th Int. Symp. Power Semicon. Devices & Ics, 2007,p. 17

Summary

- Csuprem+Apsys (2/3D) includes the proper models for HV devices.
- 2/3D simulation of HV MOSFET turns out to be efficient and stable for both off and on states, with or without floating gates.
- Reasonable physical trends demonstrated for LDMOS.
- 3D simulation compared with 2D to show interesting results relating to use of floating gates in HV MOSFET.
- 3D simulation of hybrid IGBT shows pronounced 3D effects.

Acknowledgement: C. Wu and J. Gong of NTHU (Taiwan) contributed some figures in this presentation.