Advanced 3D TCAD Simulation of Semiconductor Devices

Crosslight Software, Inc., Burnaby, Canada

Introduction–TCAD

What is TCAD?

- Technology Computer Aided Design for semiconductor devices

Why TCAD?

- TCAD is critical for semiconductor device industry, both discrete and integrated
- It saves time and money, provides deep understanding of the physics

Why 3D TCAD?

- More realistic
- Device nature requires 3D (i.e. Superjunction Power Device, CIS)

About Crosslight Software, Inc.

A Canadian company with a history of more than 15 years

1998

Laser Focus World

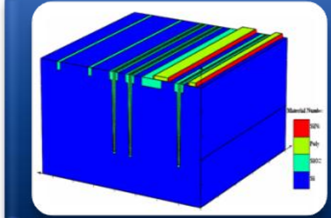
Commercial Technology Achievement Award

Crosslight Software Inc.

Gloucester, Ontario, Canada

PICS3D Photonic Integrated Circuit Simulator in 3D

A pioneer and global leader of optics and photonics TCAD



A fast growing TCAD provider for silicon devices

Crosslight TCAD Products Family

APSYS
(Device Simulator)

CSuprem
(Process Simulator)

2D/3D
TCAD

PICS3D

(Photonic IC
Simulator)

LASTIP

(Laser Diode)

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Introduction to 3D TCAD Simulation

Time is the Money! Efficiency is the Key!

- Traditionally 3D bulk TCAD is time consuming, may take even longer than real fabrication time
- Not Acceptable for today's semiconductor industry

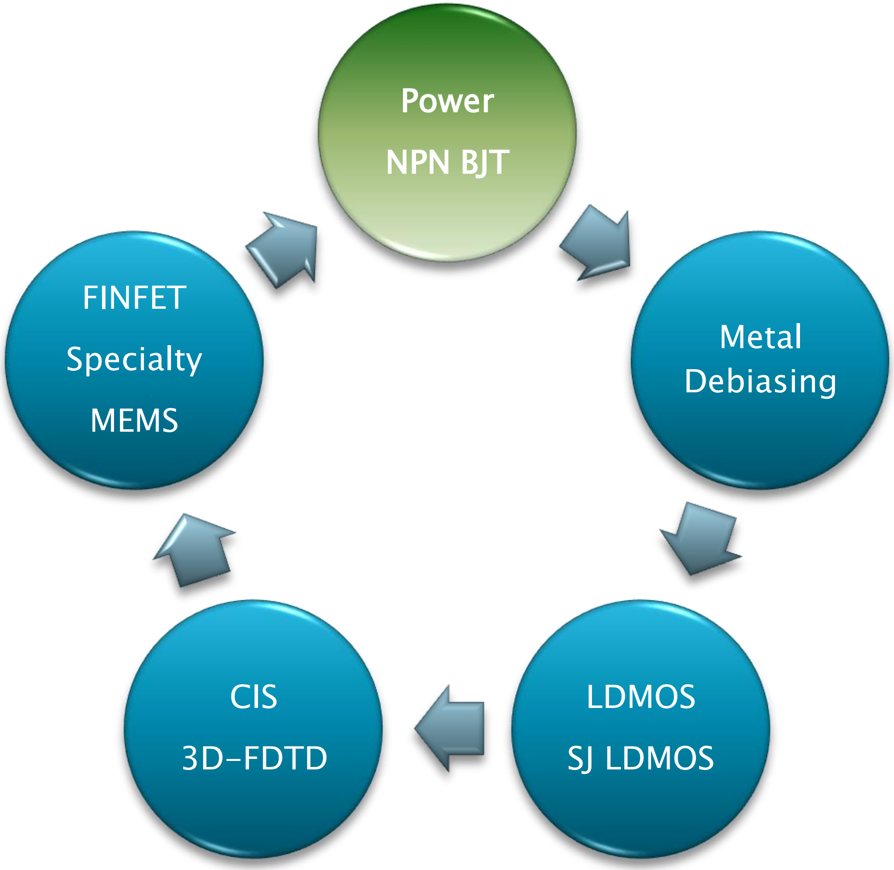
Crosslight's New Approach

- Instead of bulk simulation, Crosslight adopted a new way to stack the 2D planes in the z direction to ensure efficiency and accuracy

Quasi-3D vs. Full 3D

- Quasi-3D neglects the inter-plane dopant diffusion to save time at first, when everything is ok, full 3D will take account all the plane to plane interaction

Examples List: (With a special focus on Power Semiconductor Devices)


Power
NPN BJT

Metal Debiasing

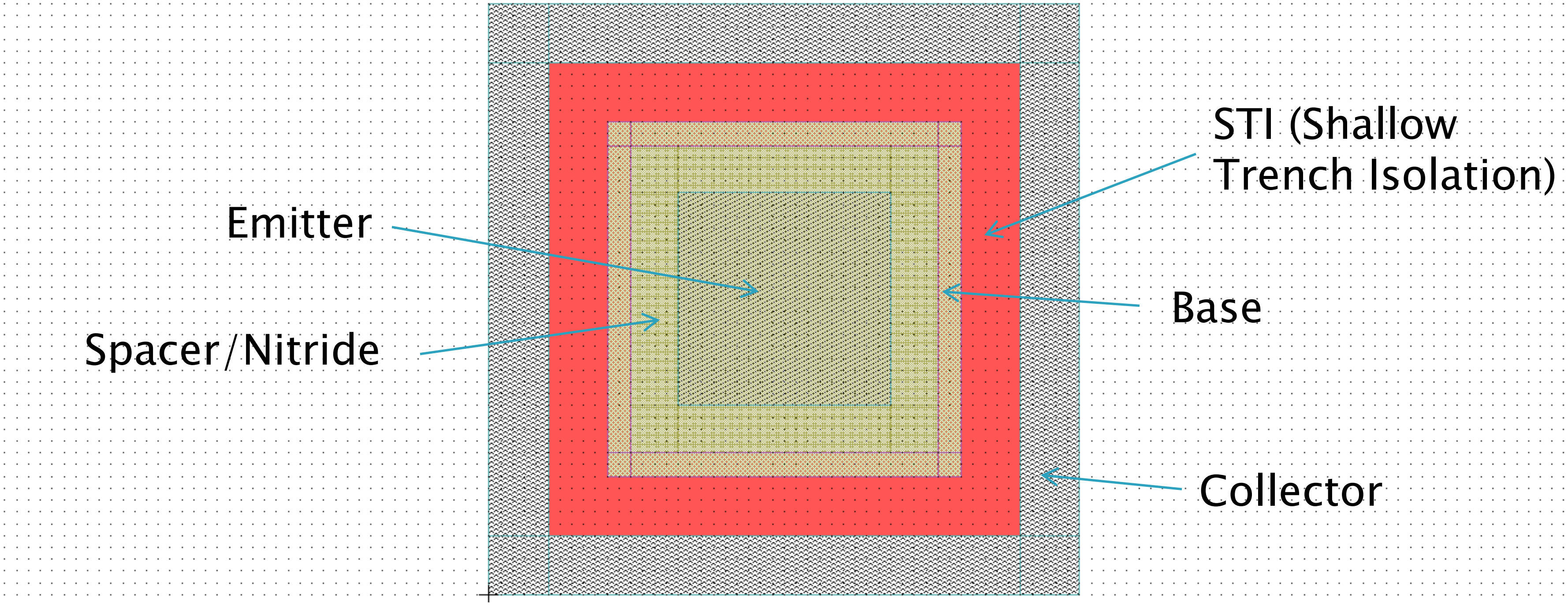
LDMOS
SJ LDMOS

CIS
3D-FDTD

FINFET
Specialty
MEMS

3D Simulation Process Build Up

- We use a vertical power NPN BJT as an example. From layout, generate the GDSII file



BEOL is neglected for simplicity

3D Build Up: Step 2

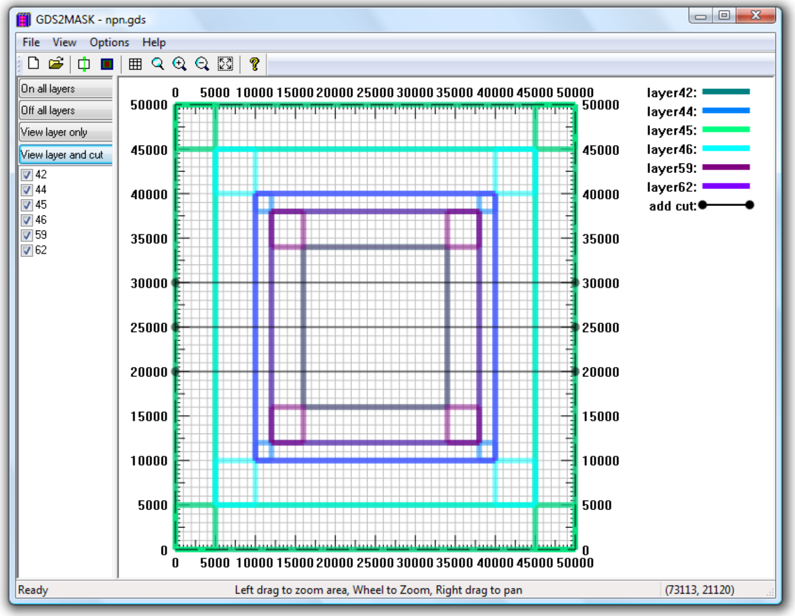
1
- Load the GDSII file

2
- Cut the layout in the z direction

3
- The .msk and .zst files are automatically generated

Z Direc. Cut(.cut file)

GDS2MASK.exe



Ready

Left drag to zoom area, Wheel to Zoom, Right drag to pan

(73113, 21120)

Mask Layers (.msk file)

Z structure (.zst file)

Crosslight provides an integrated 3D structure creation tool to simplify the 3D modeling process.

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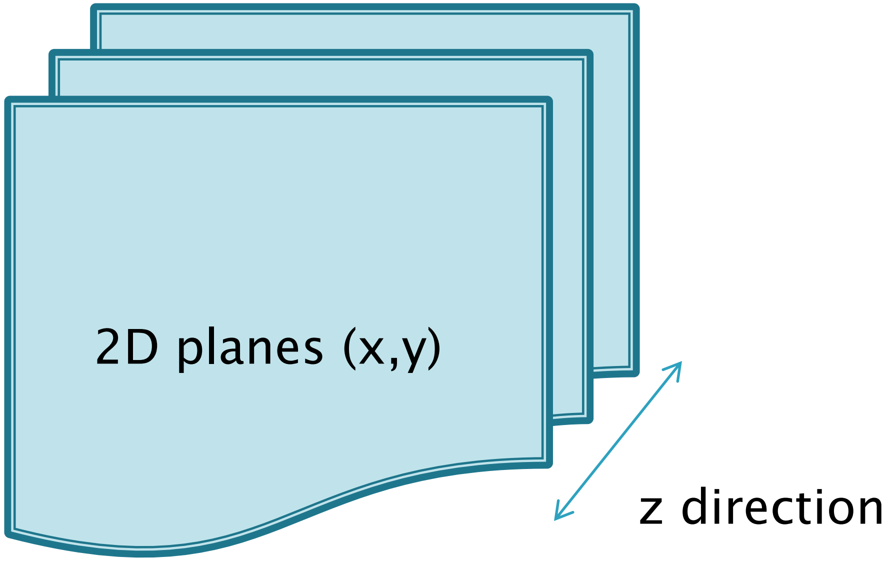
3D Build Up: Step 2 (continued)



The z structure file (.zst file) is used to control the cut location and planes in the z direction

The mask file (.msk file) is used to generate mask layers in the input file for CSuprem

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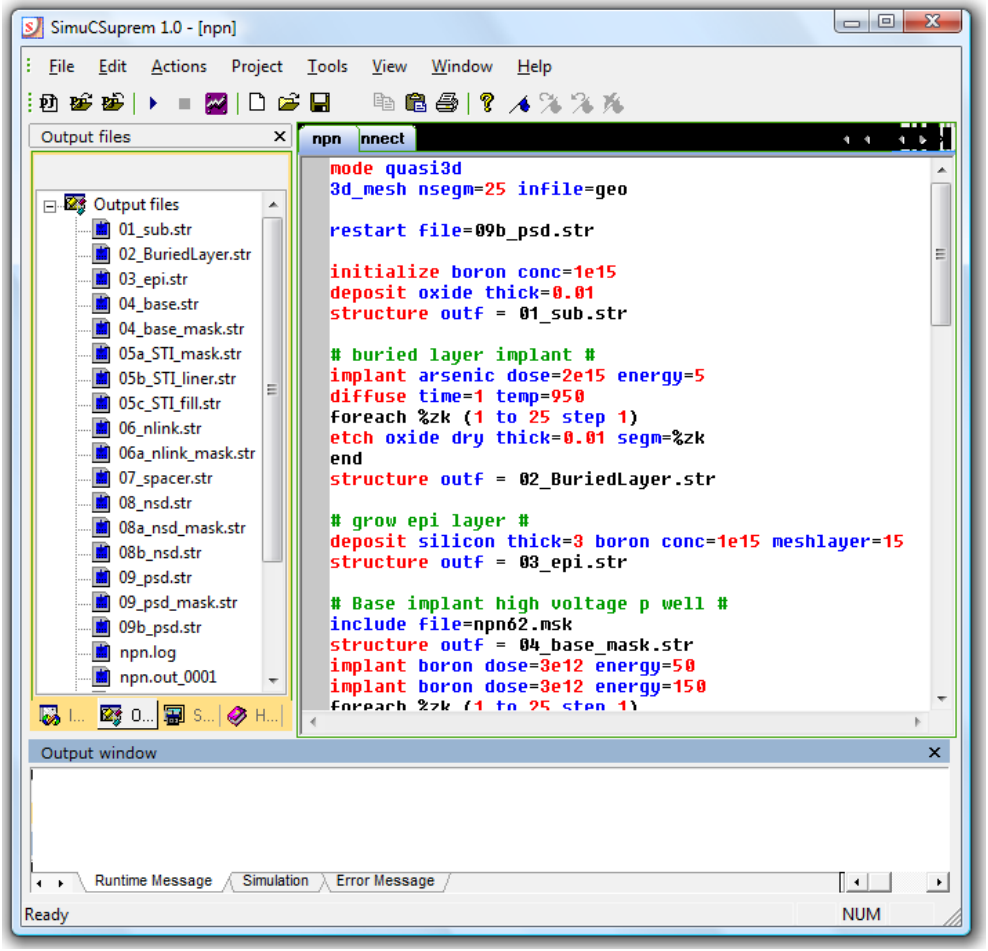
Step 3: Virtual Fabrication using CSuprem



```
mode quasi3d
3d_mesh nsegm=25 infile=geo

restart file=09b_psd.str

initialize boron conc=1e15
deposit oxide thick=0.01
structure outf = 01_sub.str

# buried layer implant #
implant arsenic dose=2e15 energy=5
diffuse time=1 temp=950
foreach %zk (1 to 25 step 1)
etch oxide dry thick=0.01 segm=%zk
end
structure outf = 02_BuriedLayer.str

# grow epi layer #
deposit silicon thick=3 boron conc=1e15 meshlayer=15
structure outf = 03_epi.str

# Base implant high voltage p well #
include file=npn62.msk
structure outf = 04_base_mask.str
implant boron dose=3e12 energy=50
implant boron dose=3e12 energy=150
foreach %zk (1 to 25 step 1)
```

CSuprem is Crosslight's version of SUPREM IV, originally developed by the Stanford University.

You can choose from quasi 3 dimensional or full 3D simulation, quasi3d means the diffusion between the z planes is not considered to boost up speed

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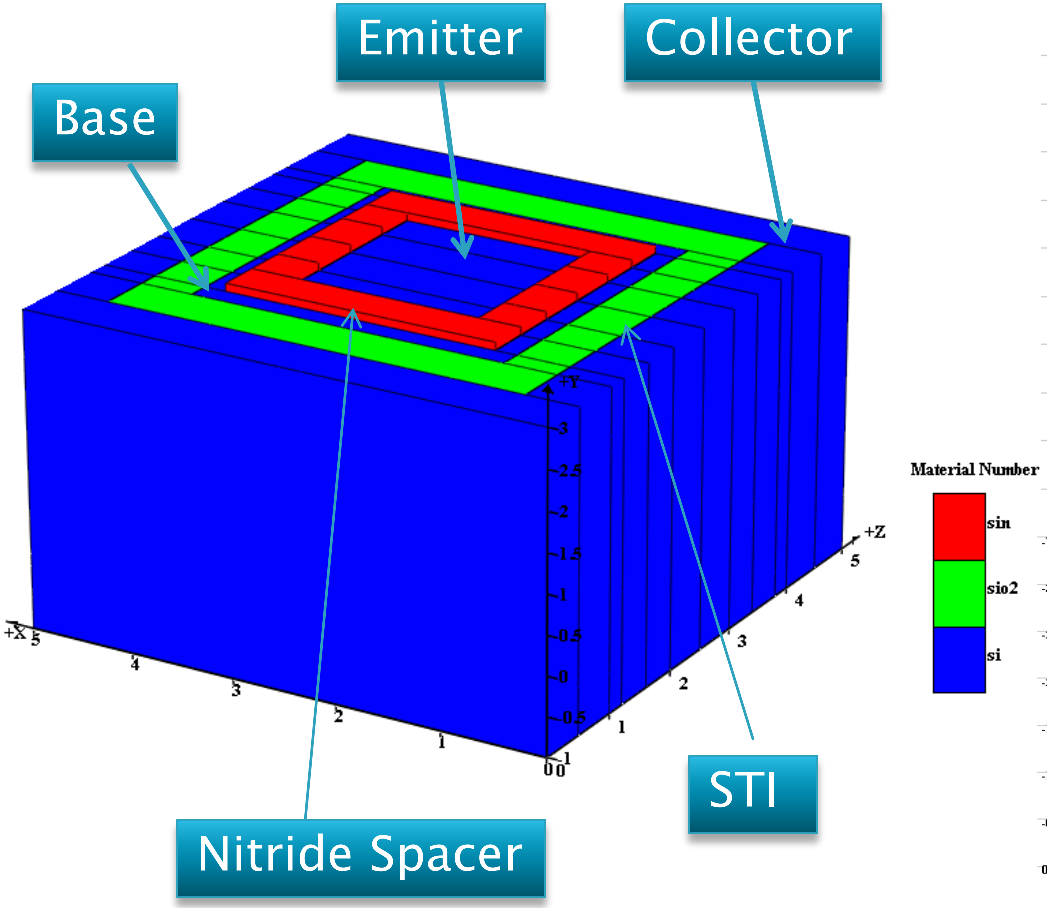
3D NPN BJT Process Simulation



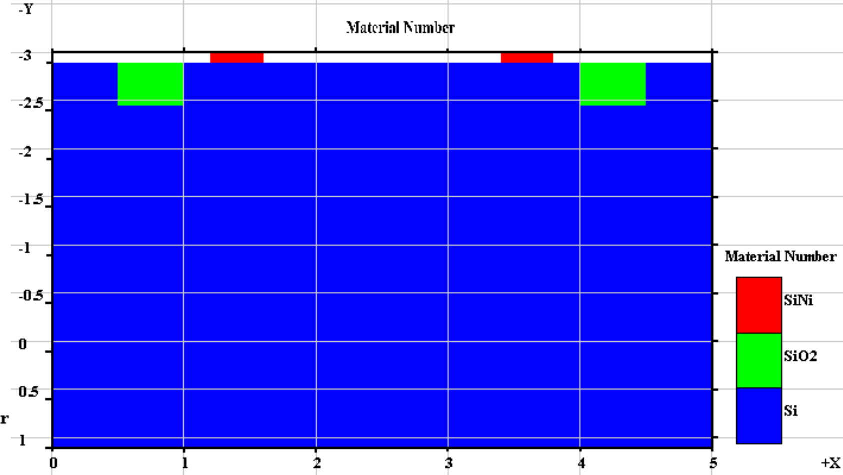
Base

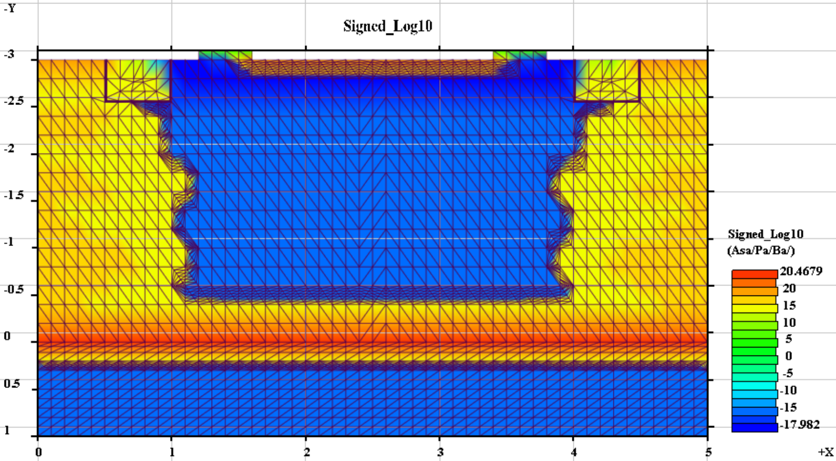
Emitter

Collector

Nitride Spacer

STI





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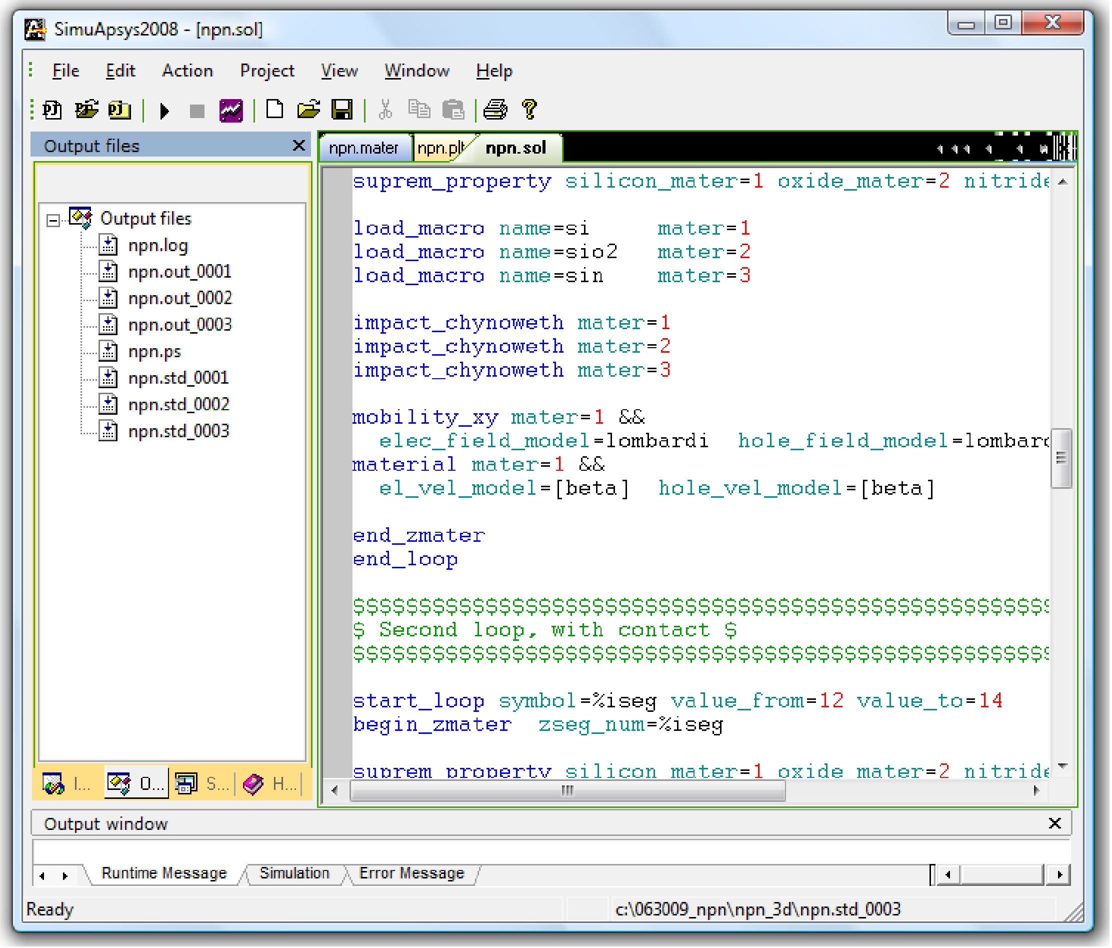
Step 4: Virtual Testing using APSYS



```
suprem_property silicon_mater=1 oxide_mater=2 nitride

load_macro name=si     mater=1
load_macro name=sio2   mater=2
load_macro name=sin    mater=3

impact_chynoweth mater=1
impact_chynoweth mater=2
impact_chynoweth mater=3

mobility_xy mater=1 &&
  elec_field_model=lombardi  hole_field_model=lombard
material mater=1 &&
  el_vel_model=[beta]  hole_vel_model=[beta]

end_zmater
end_loop

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$ Second loop, with contact $
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

start_loop symbol=%iseg value_from=12 value_to=14
begin_zmater  zseg_num=%iseg

suprem_property silicon_mater=1 oxide_mater=2 nitride
```

Advanced Physical Models of Semiconductor Devices, is based on 2D/3D finite element analysis of electrical, optical and thermal properties of the semiconductor devices, with silicon as a special case.

APSYS

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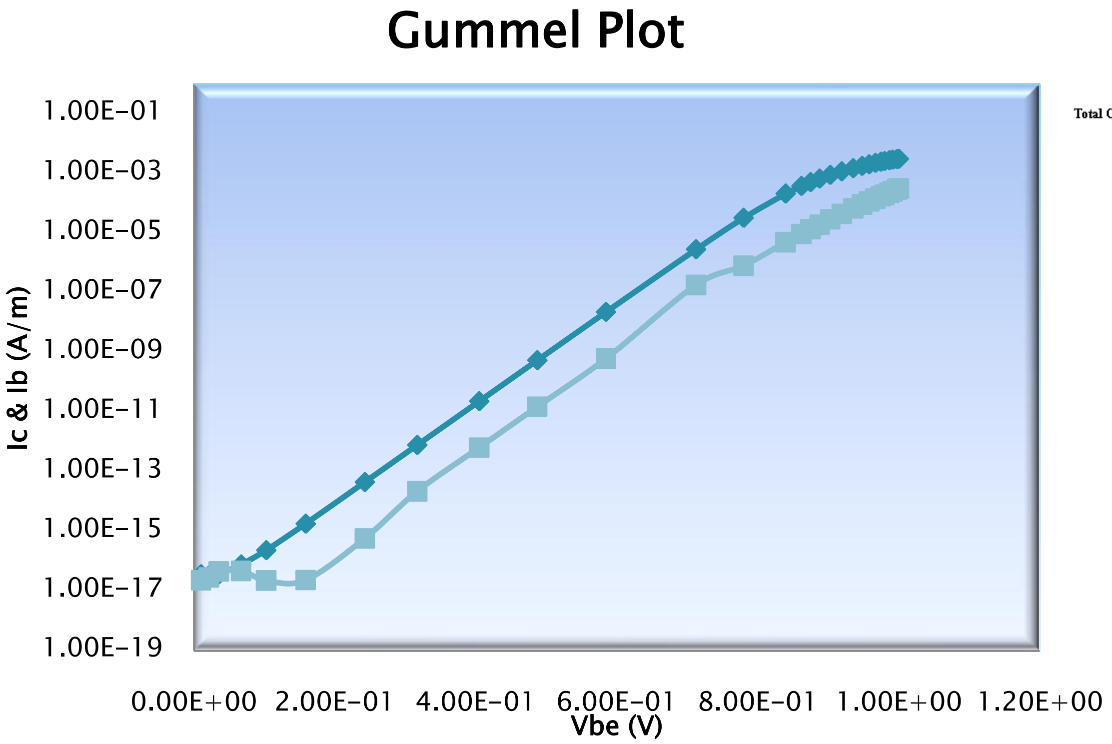
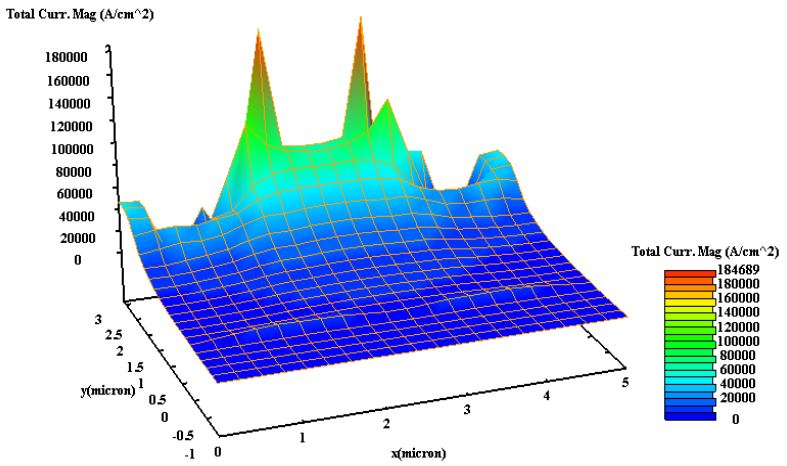
Device Simulation Result of 3D NPN BJT



Gummel Plot



2D center cut: Total (electron and hole) Current Contour Plot

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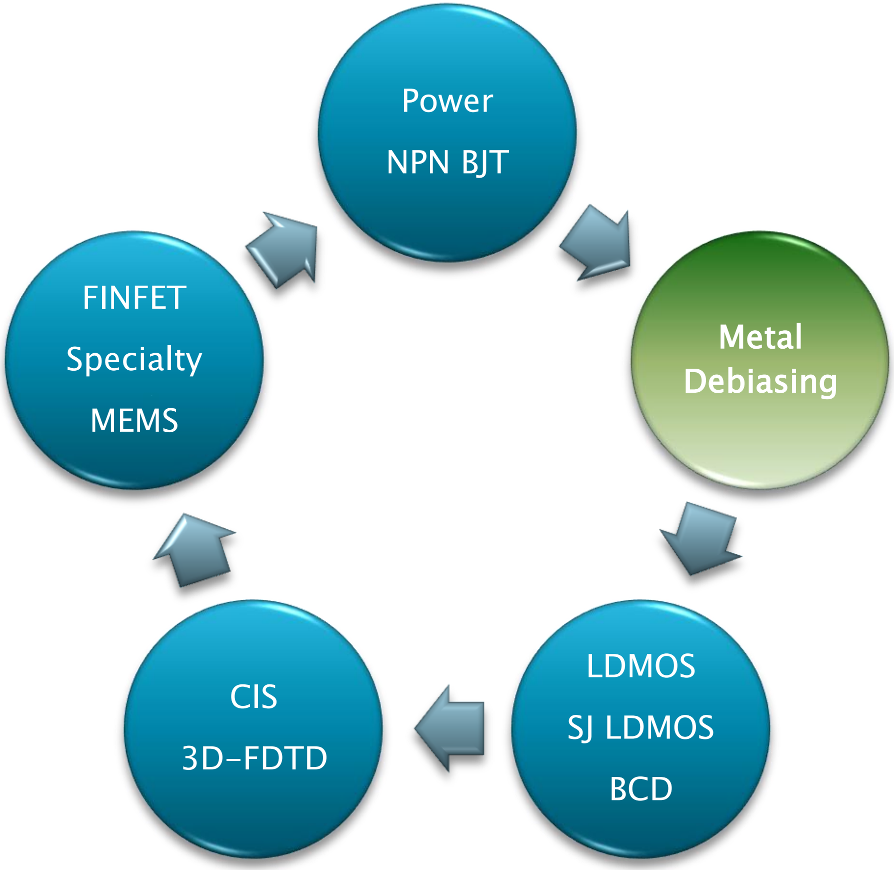
Examples List:



Power

NPN BJT

Metal Debiasing

LDMOS

SJ LDMOS

BCD

CIS

3D-FDTD

FINFET

Specialty

MEMS

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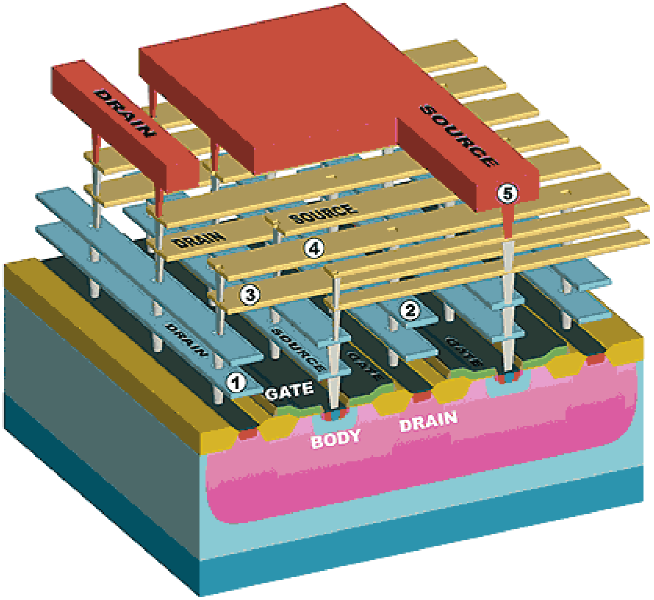
Interconnect Metal Debiasing :

A well known problem for the Power IC Industry



The BCD6 high-voltage LDMOS FET uses five interdigitated aluminum/copper metal levels. While the first four layers contact the drain and source fingers, the fifth level carries the current to the pads. Replacing the fifth layer, which is 3 µm thick, with a 5-µm copper layer improved the metal contribution to the on-resistance of the power LDMOS by 60%.

LDMOS from ST

Huge Size! Metal Resistant is no longer negligible

- Metal resistant comparable to device Rdson
- Different metal pattern will yield different Res.

Lump model is not good

- 3D nature, too complicated to model using lump elements.

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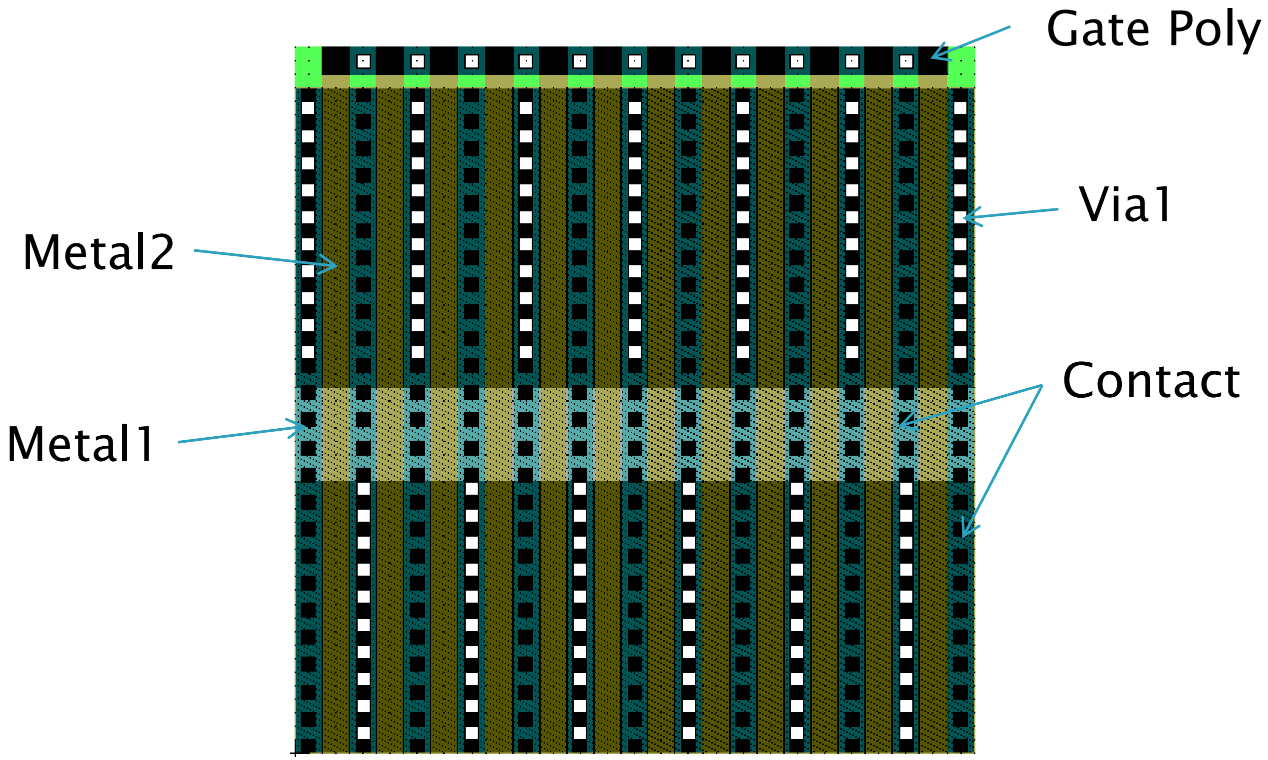
Layout of Metal Interconnect

- The metal interconnect for large sized power MOSFET generally contribute to considerable amount of total resistance, a 3D model is generally necessary to determine the resistance from the metal lines.

- Layout:



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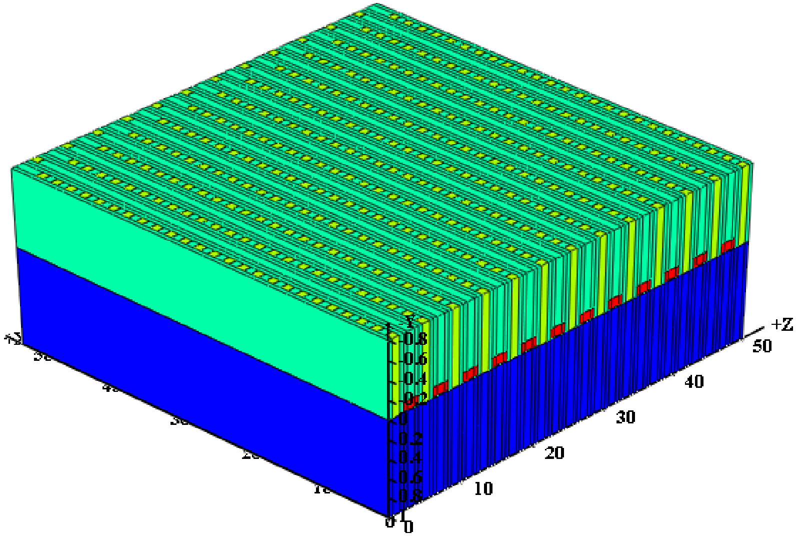
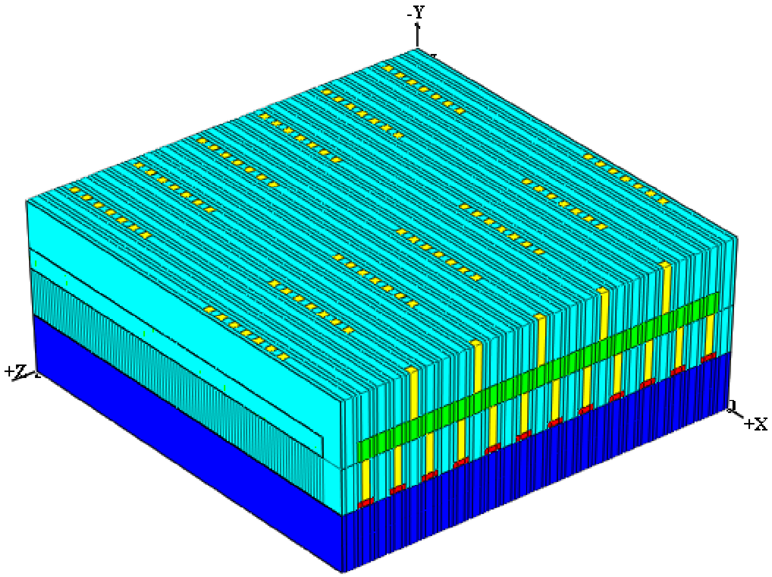
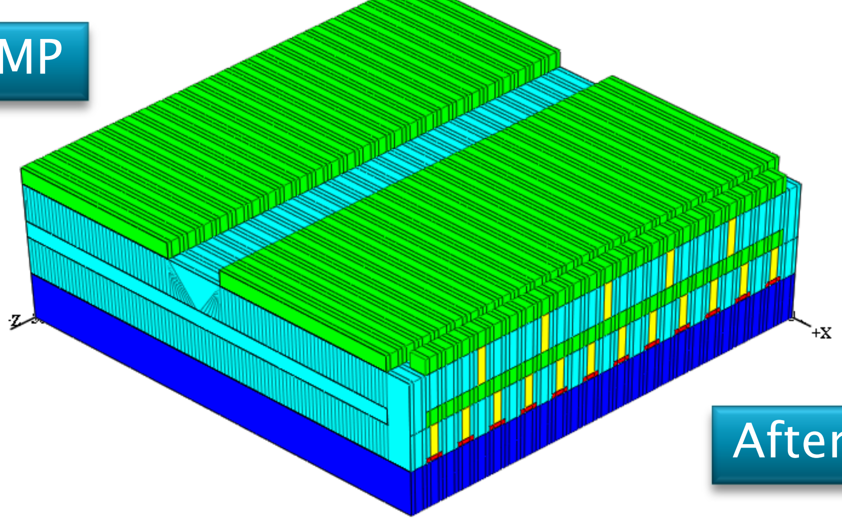
Process Simulation of Metal Interconnect



After Contacts CMP



After Via1 CMP



After Metal2 CMP

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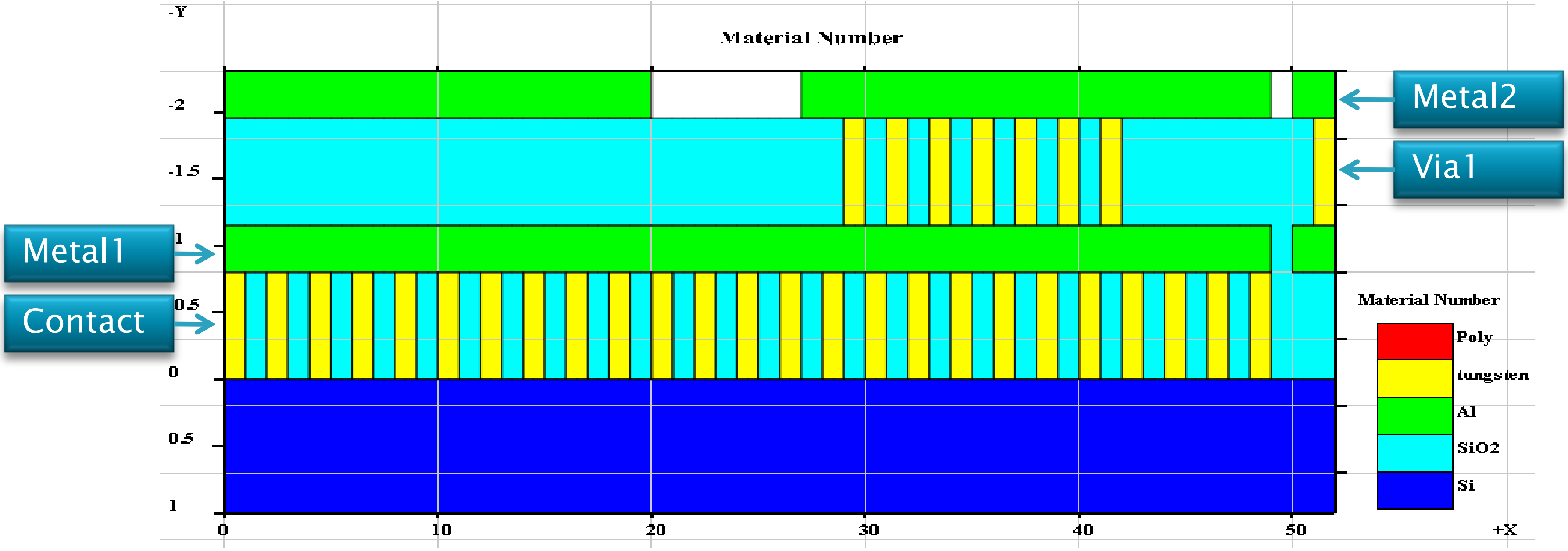
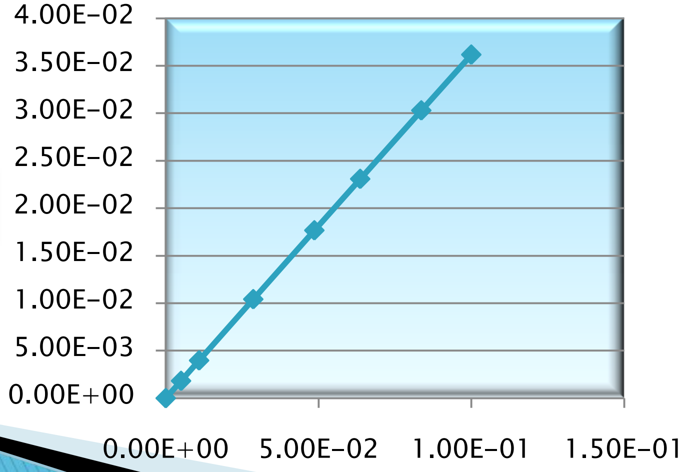
2D Cut and Device Simulation



2D cut from center

I-V Curve



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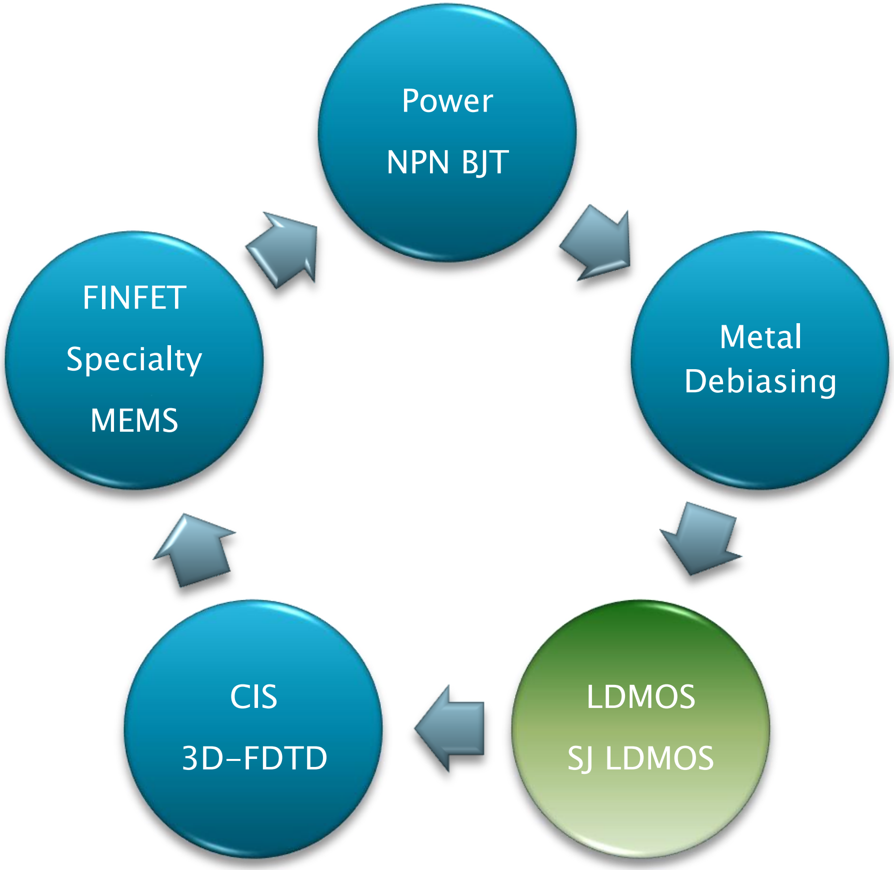
Examples List:



Power

NPN BJT

Metal Debiasing

LDMOS

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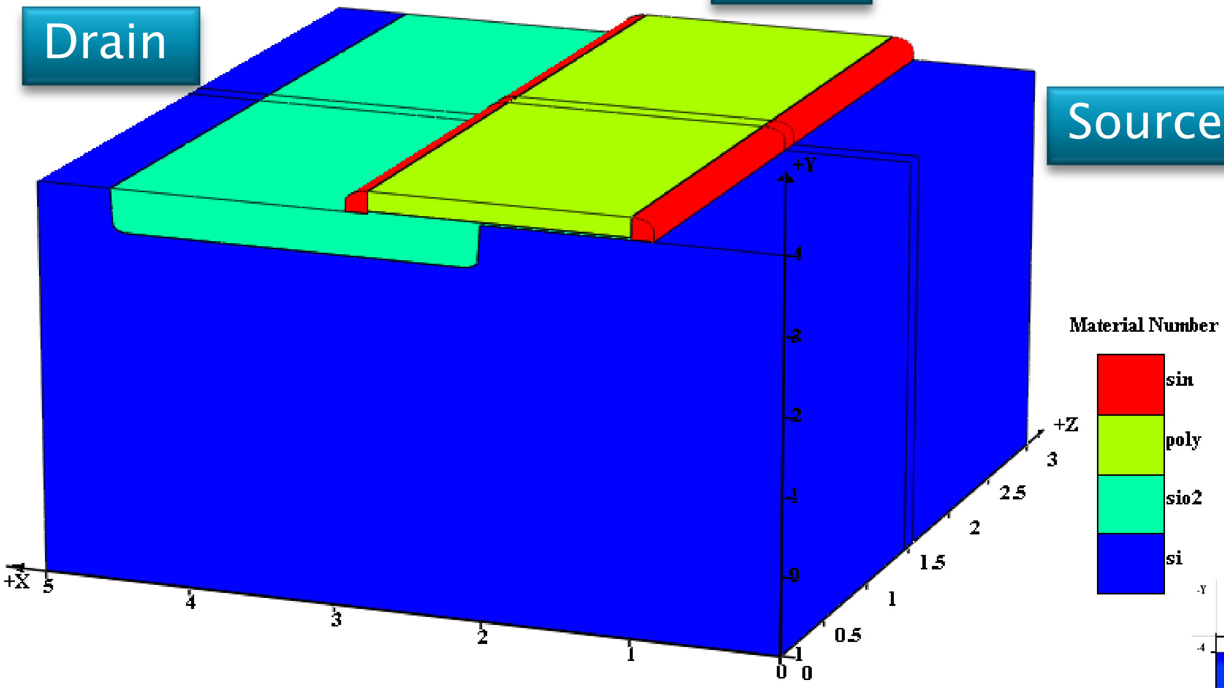
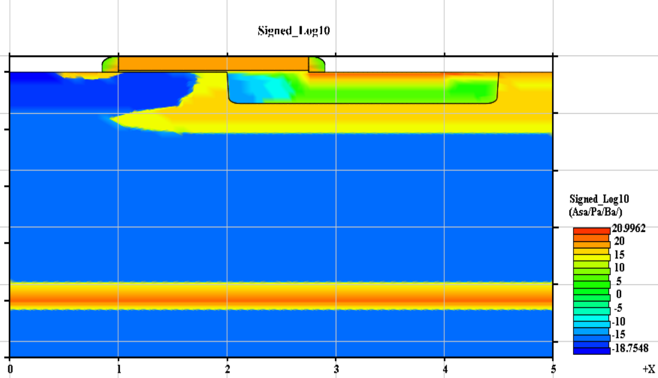
Power LDMOS Process Simulation



Drain

Gate

Source



2D cut:
Net Doping

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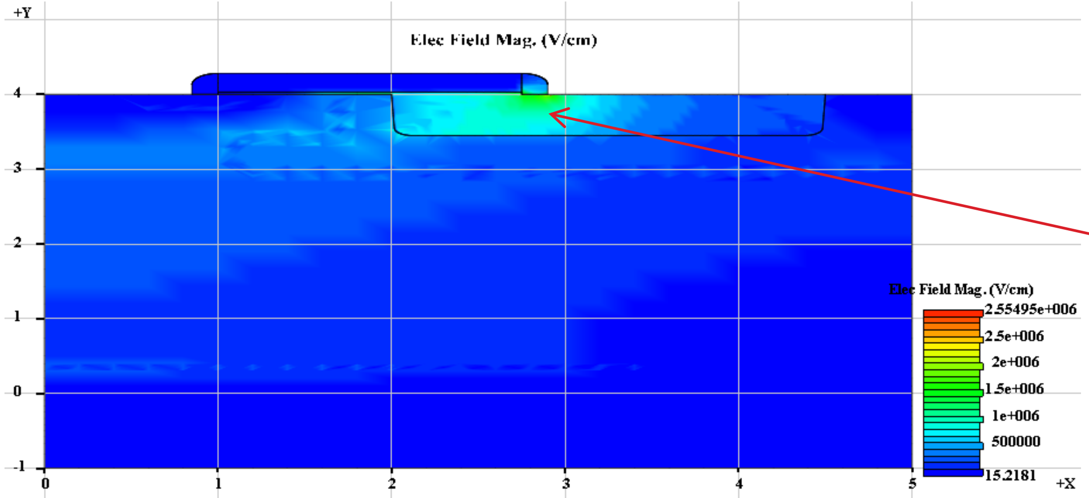
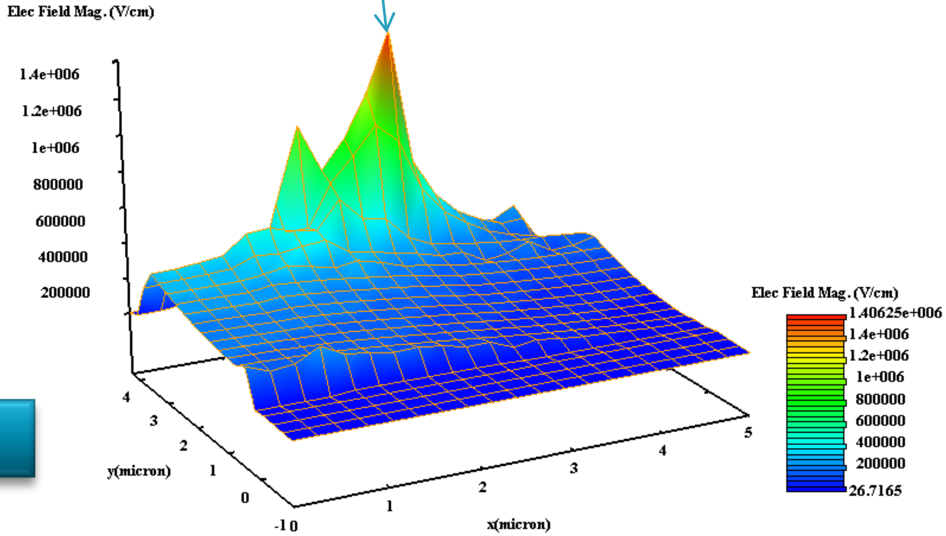
Power LDMOS Device Simulation



Highest Electric Field is located under gate edge in the STI, other areas are pretty flat

2D cut: Electric Field



Contour Plot of E. Field

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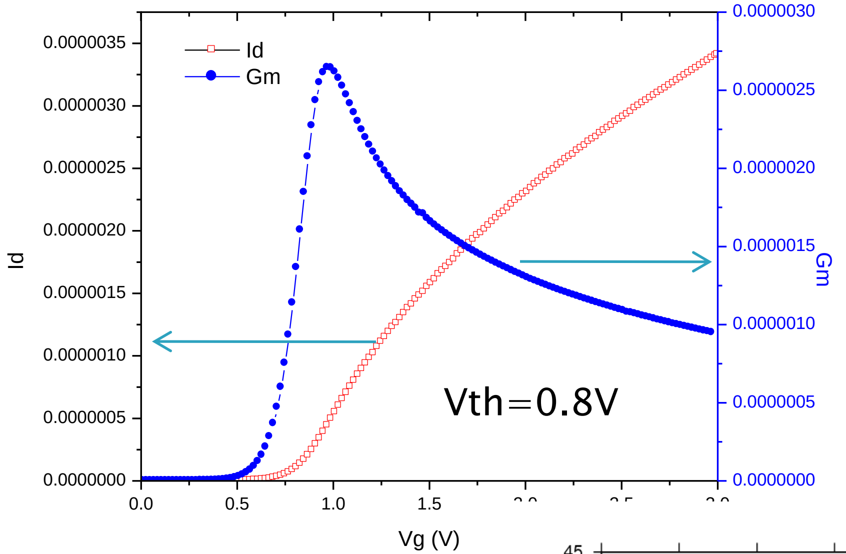
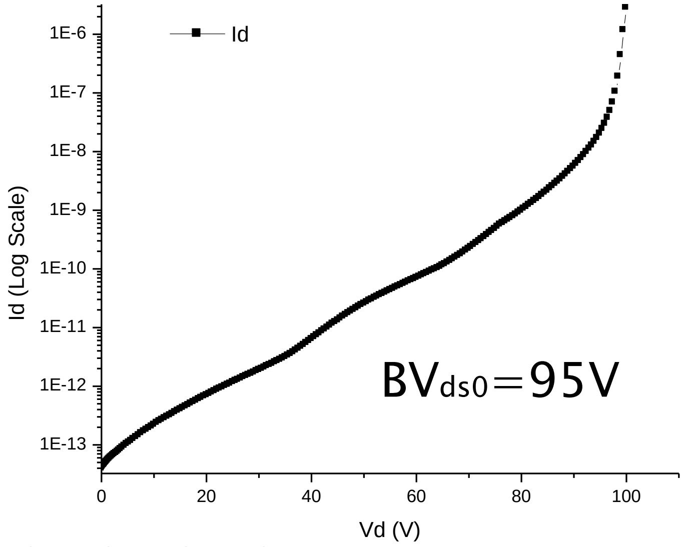
3D Device Simulation of Power LDMOS

Threshold and Transconductance



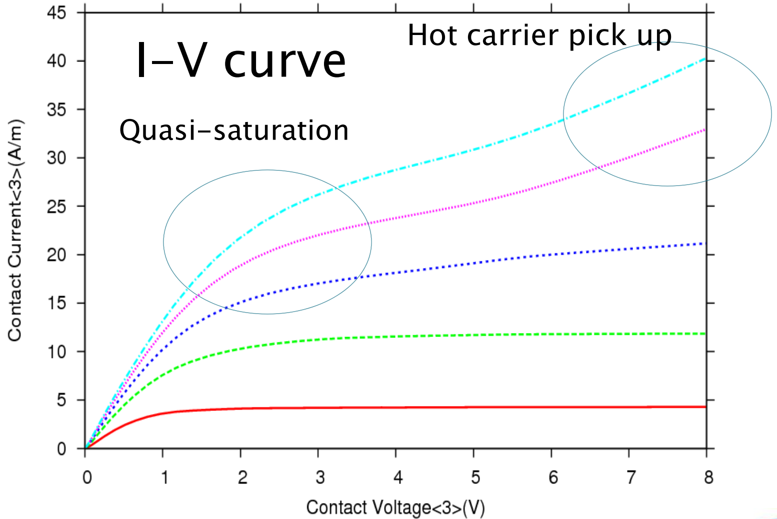
Vth=0.8V

Reverse Breakdown



BV_{ds0}=95V

File:Ron.plt



I-V curve

Quasi-saturation

Hot carrier pick up

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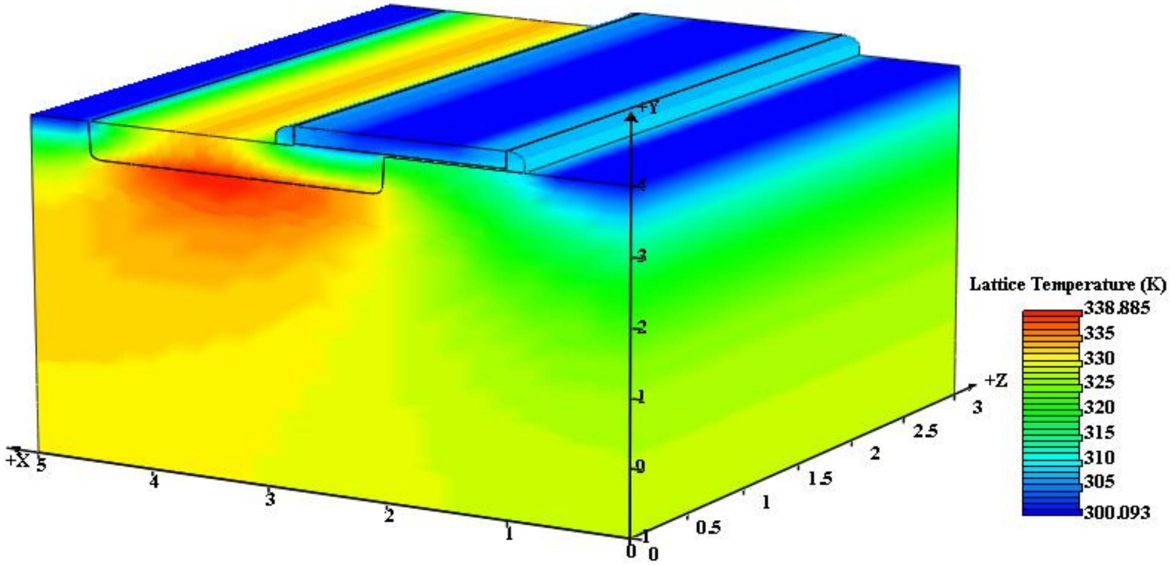
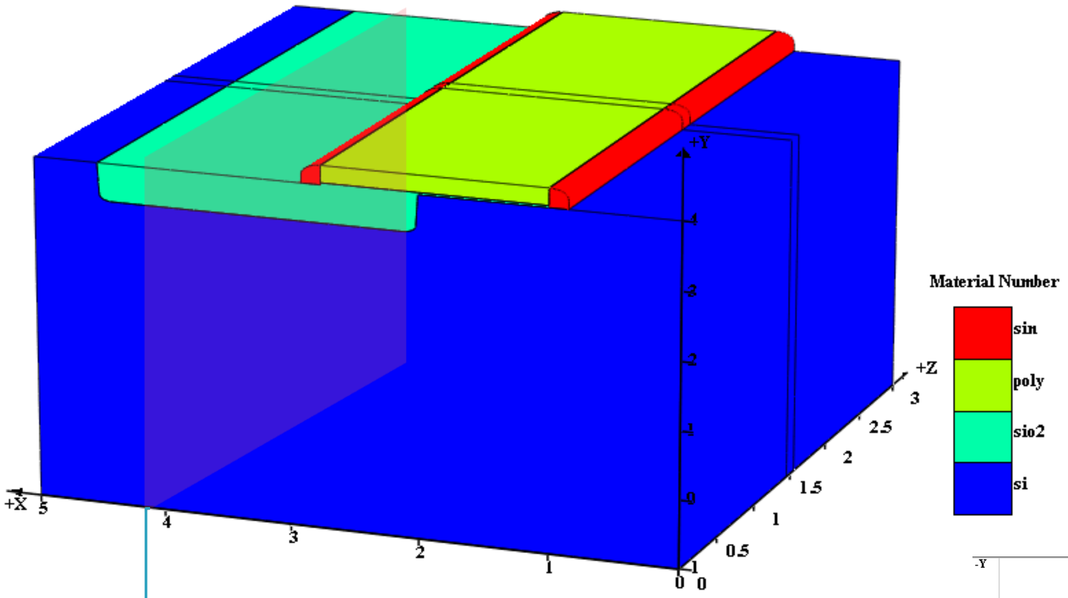
Device Self-Heating and Thermal Simulation

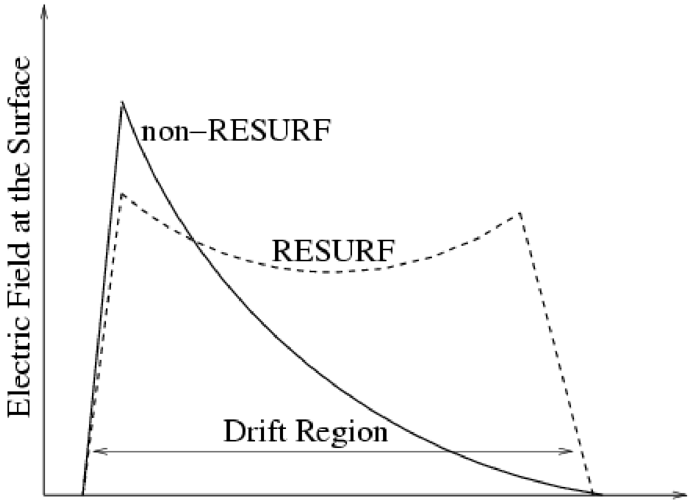


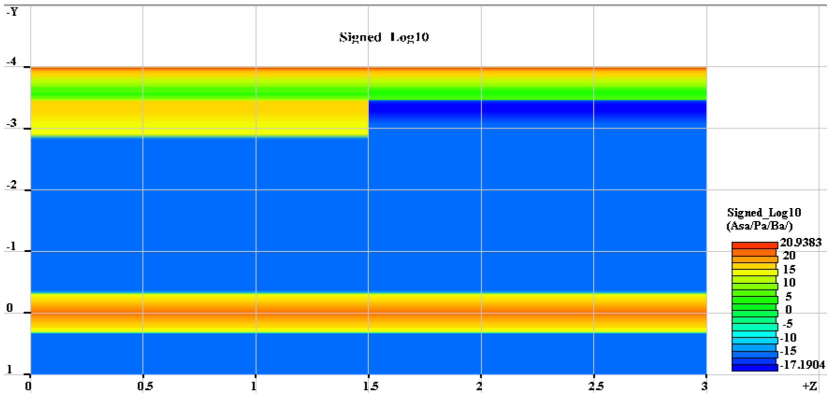
Vg=12V
Vd=55V
Self Heating with thermal conductance of 0.1 W/mK

3D Superjunction LDMOS Process Simulation



2D cut to Show Net Doping





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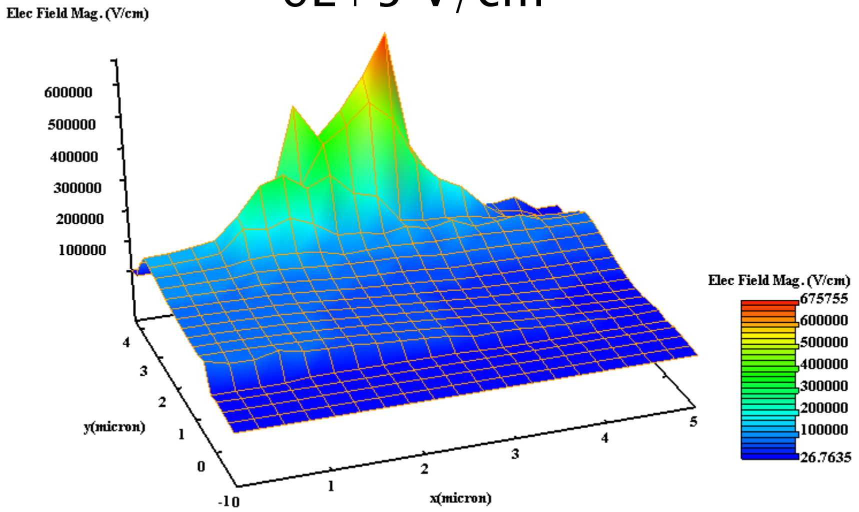
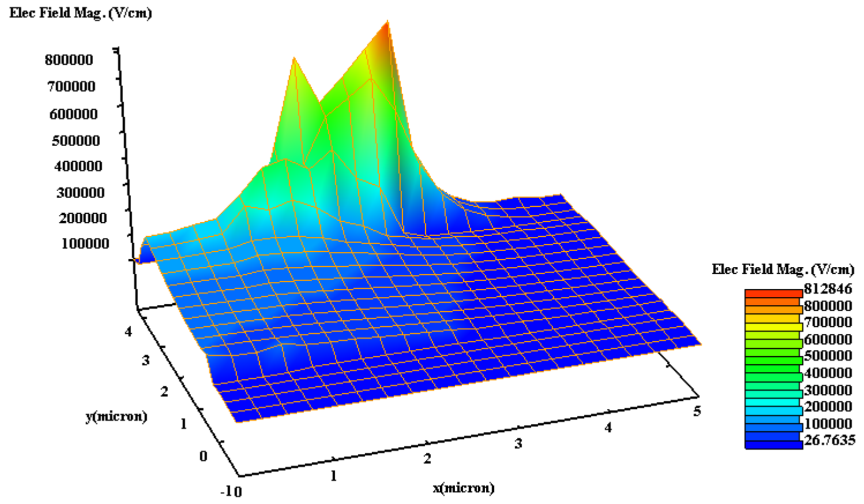
Comparison of Surface Electric-field

6E+5 V/cm



SuperJunction LDMOS

8E+5 V/cm



Normal LDMOS

Superjunction has lower Surface field than normal LDMOS with the same drain bias.

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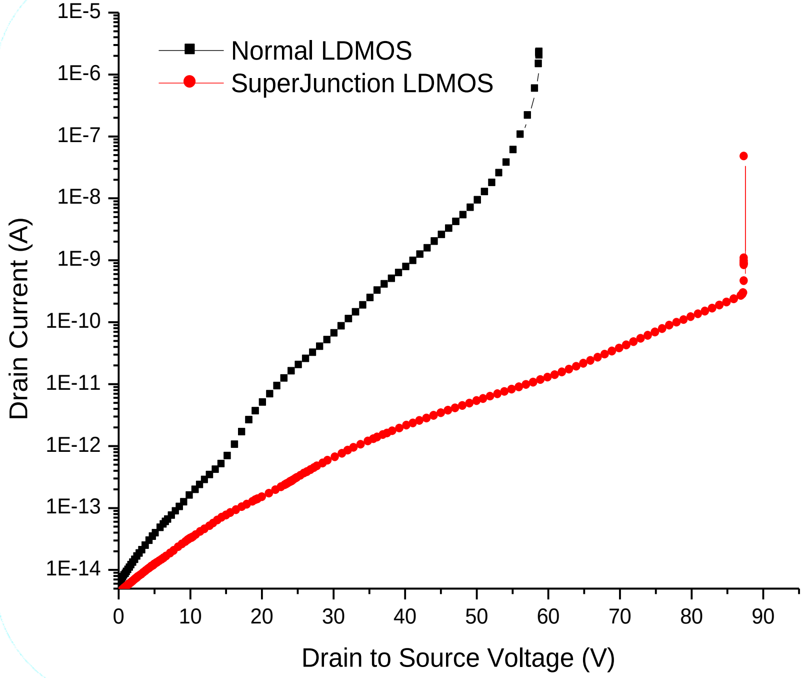
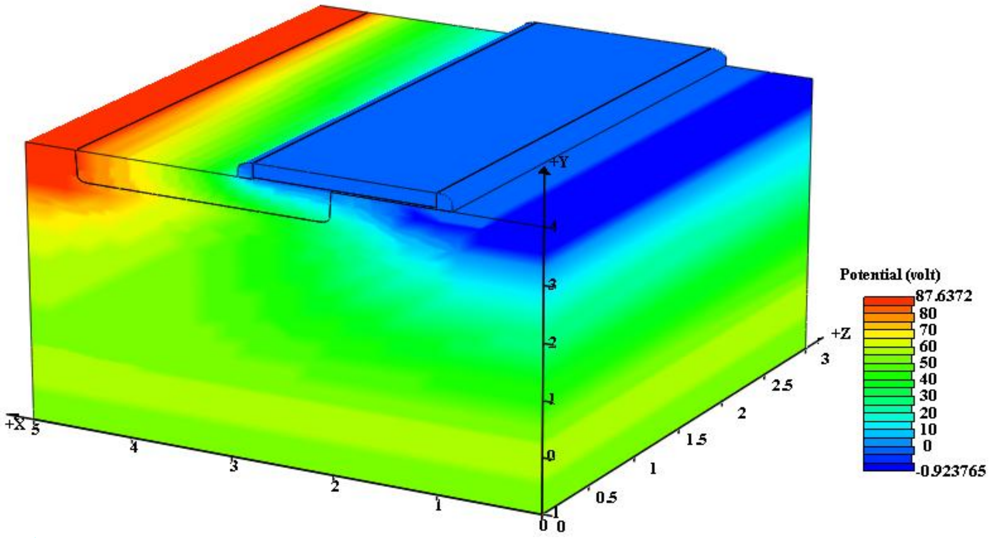
Breakdown Voltage Comparison





Comparison of Breakdown Voltage of SuperJunction LDMOS and normal LDMOS, a clear breakdown voltage increase for Superjunction LDMOS with the same process condition.

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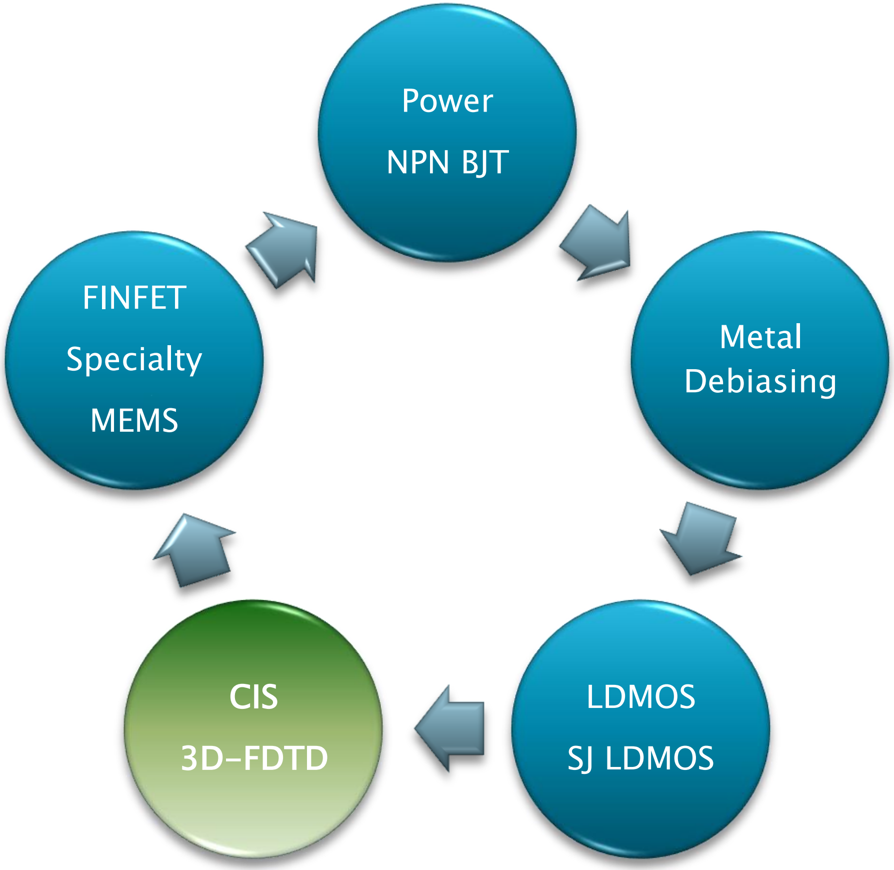
Examples List:



Power

NPN BJT

Metal Debiasing

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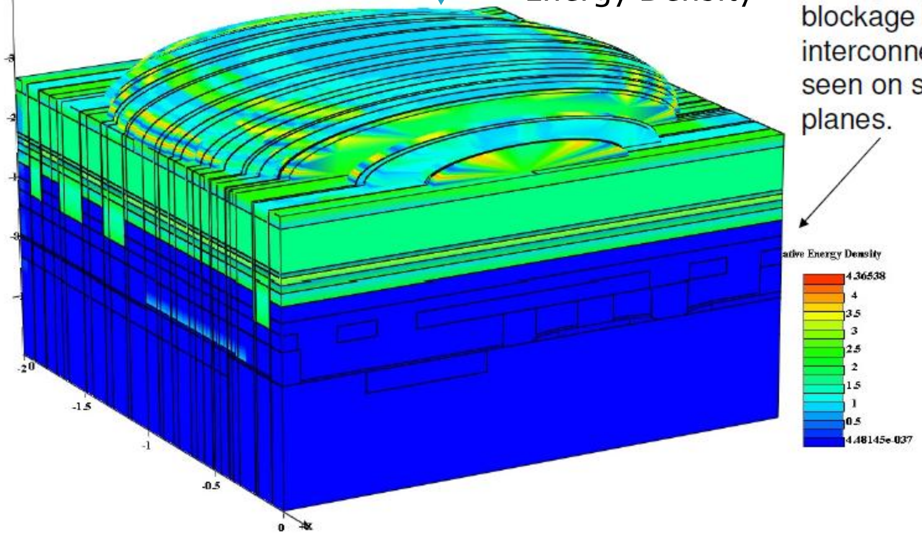
Specialty

MEMS

CMOS Image Sensor–Optical Simulation

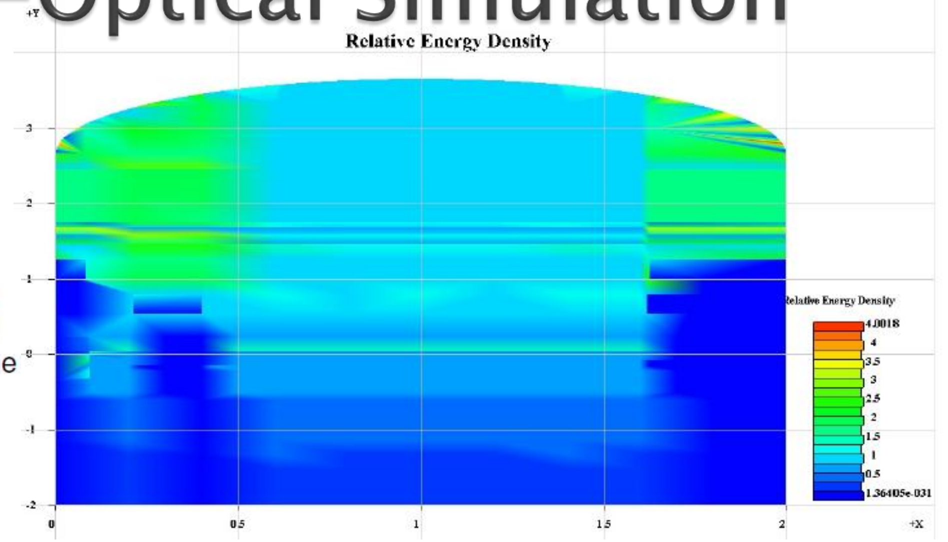
Optical Simulation 3D-FDTD



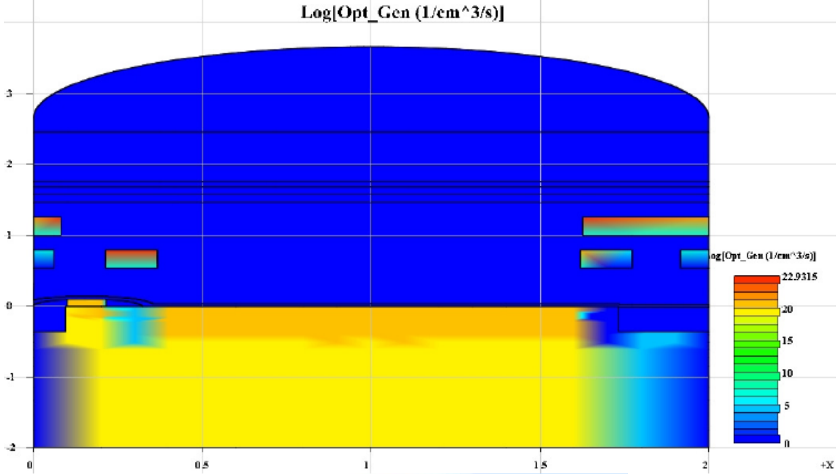
Relative Energy Density

Strong blockage by interconnect seen on some planes.

Finite-difference time-domain (FDTD) is a computational electrodynamics modeling technique, dealing with electromagnetic wave interactions with material structures.



2D-Cut of the Incident Light relative energy density



2D-Cut of the Optical Generation

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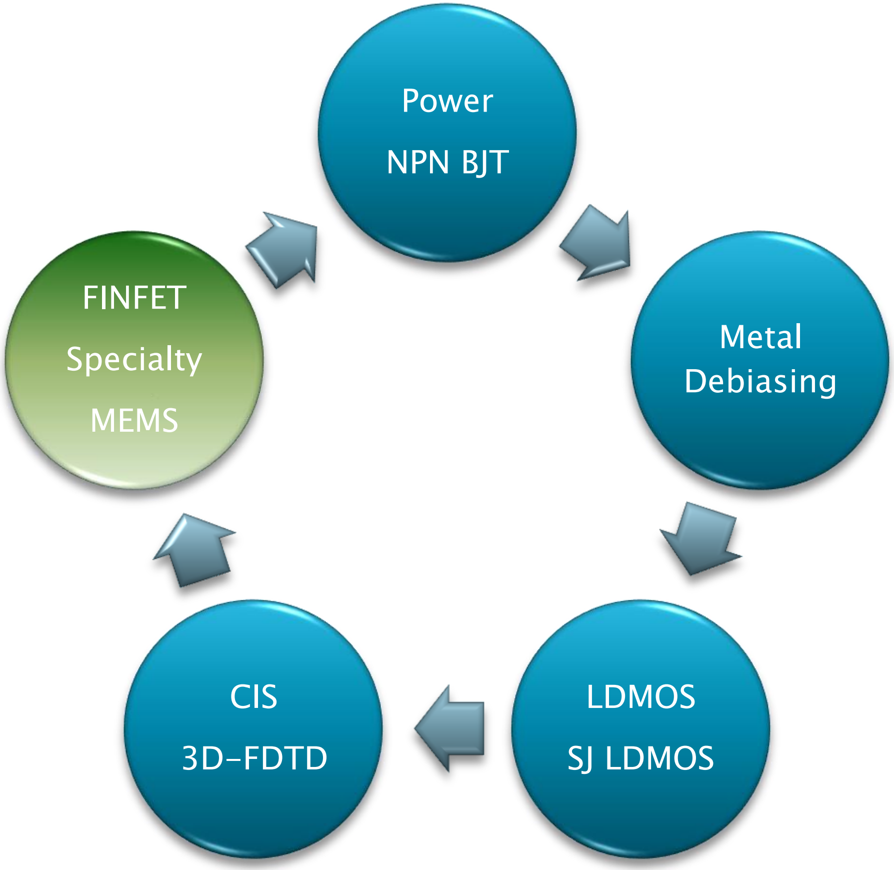
Examples List:



Power

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Metal Debiasing

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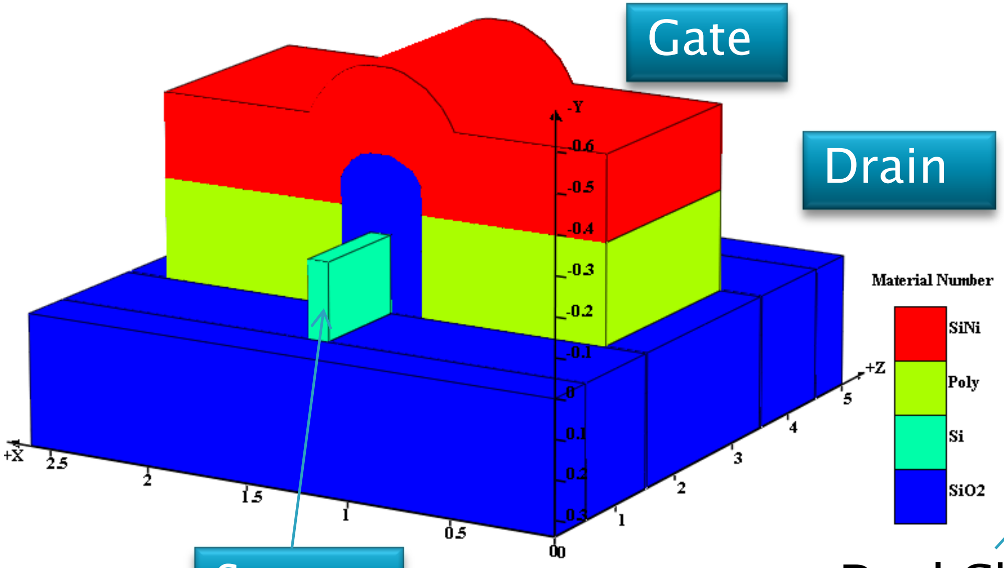
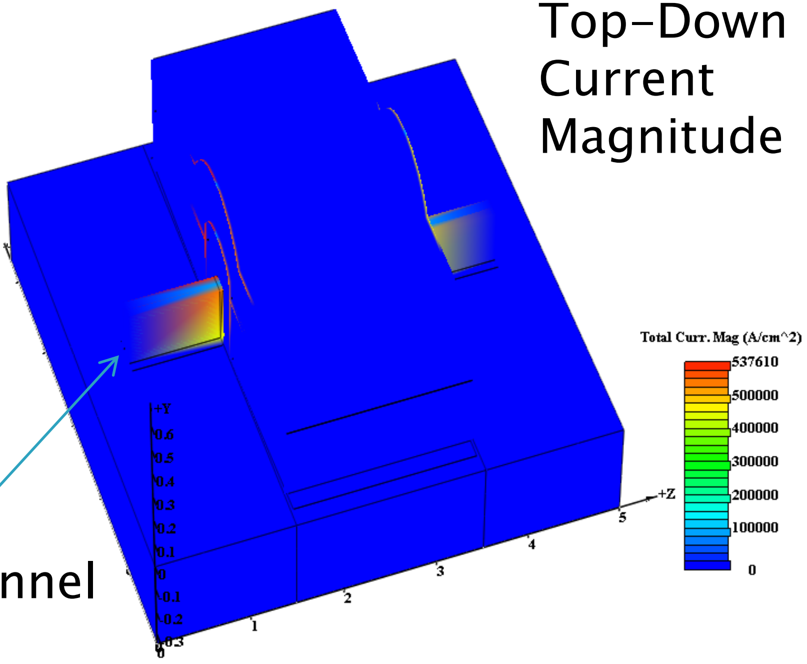
MEMS

3D Process Simulation of FINFET

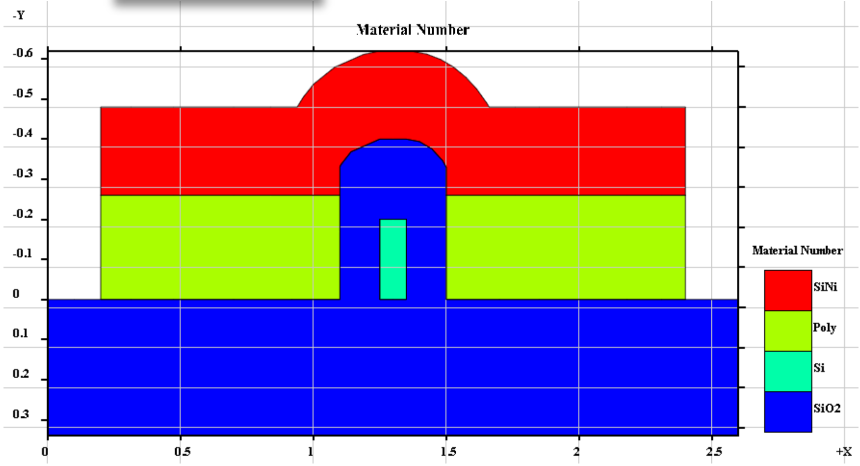


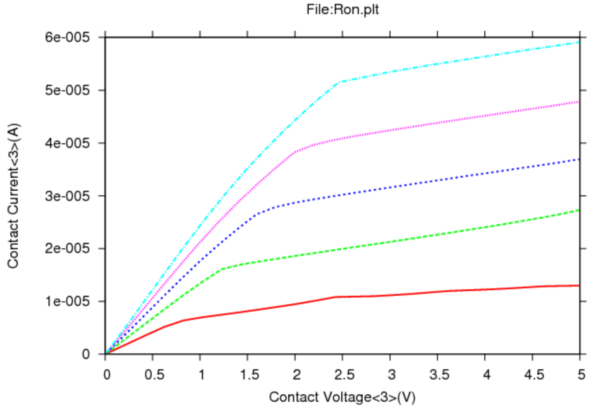
Source



Top-Down Current Magnitude

Dual Channel





I-V curve

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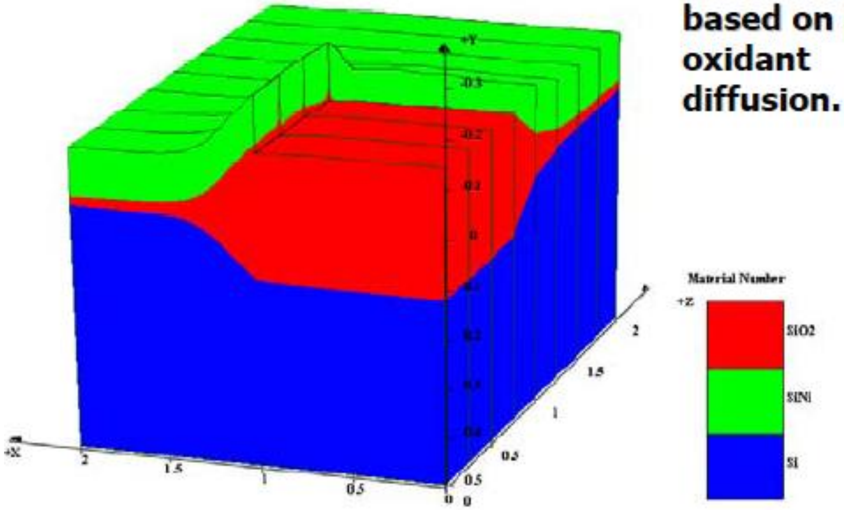
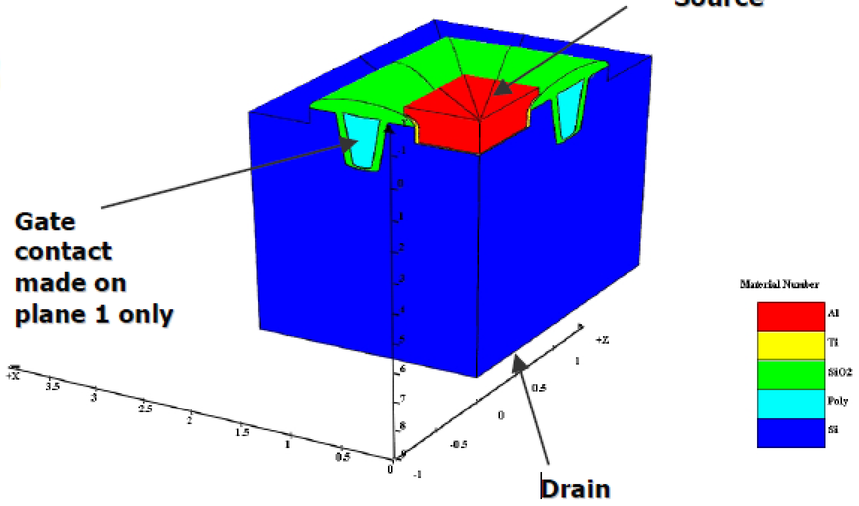
Some Other Specialty Devices

3D LOCOS growth

Field oxide growth simulation based on 3D oxidant diffusion.



UMOS with rotated planes



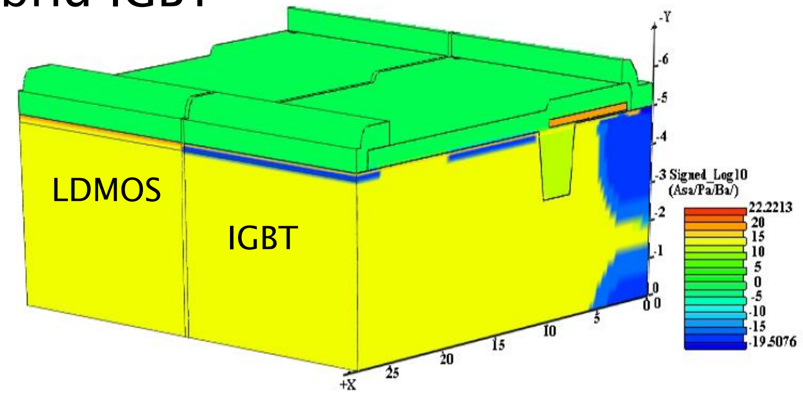
Source

Gate contact made on plane 1 only

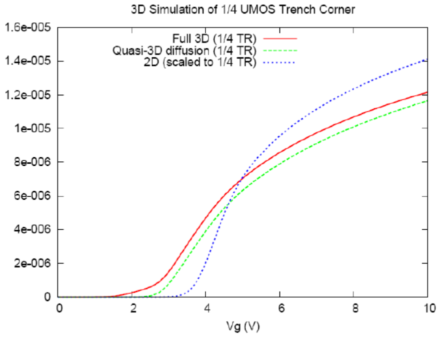
Drain

Use rotated mesh planes so that the U-shaped trench/GOX can be accurately defined for all parts of the 3D structure which is to be compared with pure 2D simulation of plane 1.

Hybrid IGBT



Comparison of Id-Vg



UMOS Id-Vg

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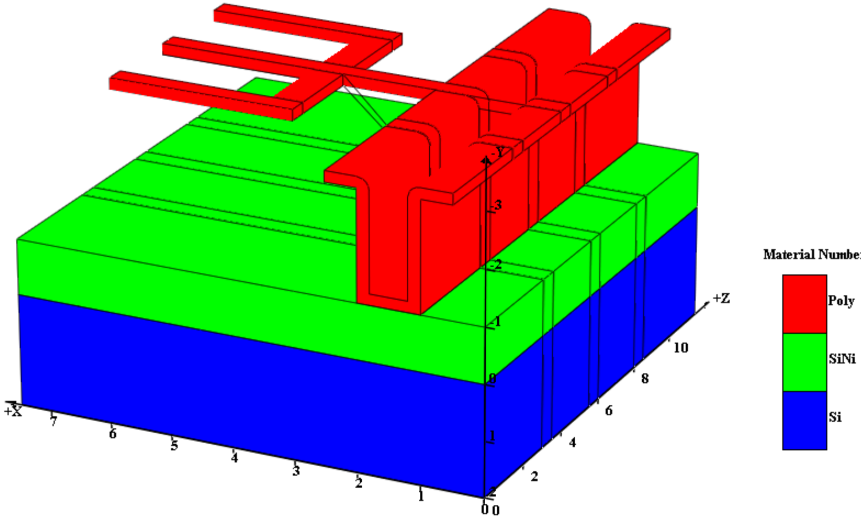
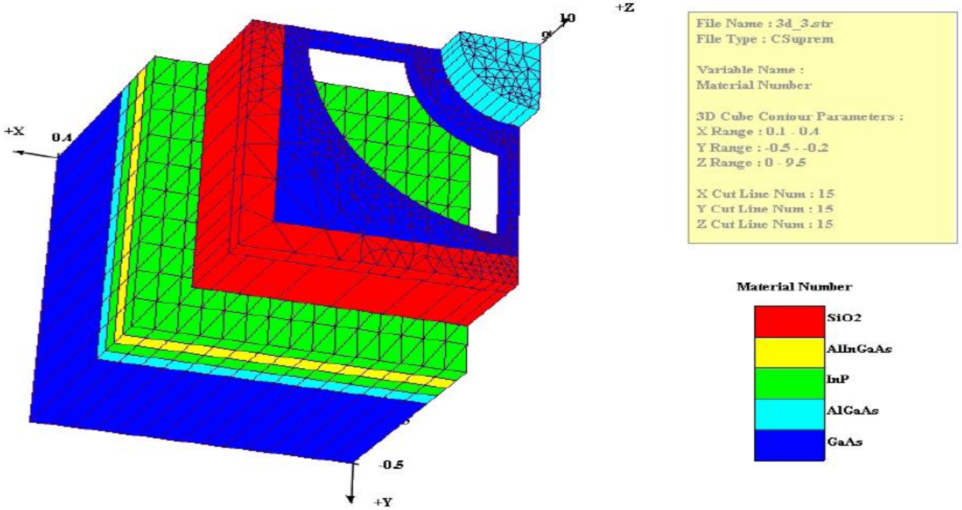
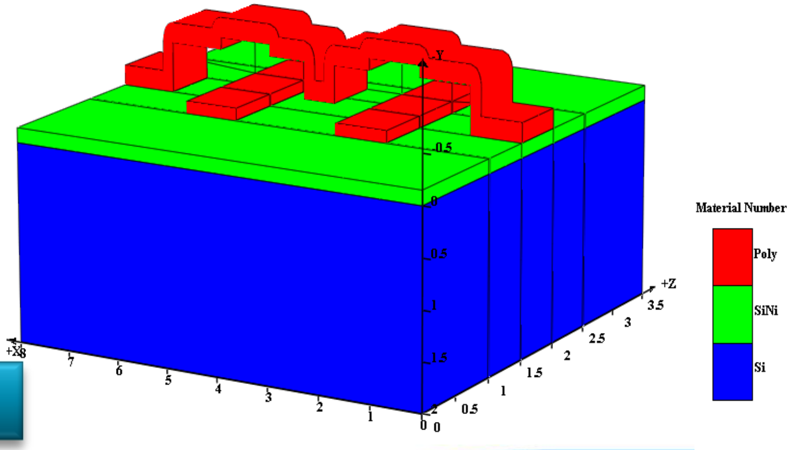
3D Process Simulation of MEMS Devices



Electro Meter



V-MEMS Tunable VCSOAs



RF Switch

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3D CSuprem Process Simulation Summary

- PC: HP Laptop with Intel Core2 P8600@2.4G Memory 6G, Video card: 512M Nvidia 9600M GT
- System: Windows Vista 64bit

	MEMS – Electrometer	MEMS–RF Switch	NPN BJT Quasi3D	NPN BJT Full3D	Metal Interconnect	SJ LDMOS Quasi3D	SJ LDMOS Full3D
Time	40s	60s	22m	40m	17m	50m	92m
Mesh	1198	1068	36455	36455	115700	79049	85931
Planes	15	5	25	25	154	33	33

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Thank You!