

*Lighting up the Semiconductor World...*

*Practical New Approach to*  

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*3D TCAD Simulations*

*By: Simon Li, Fred Y. Fu, Lisa Li and Kentaro Uehara*

# What is TCAD?

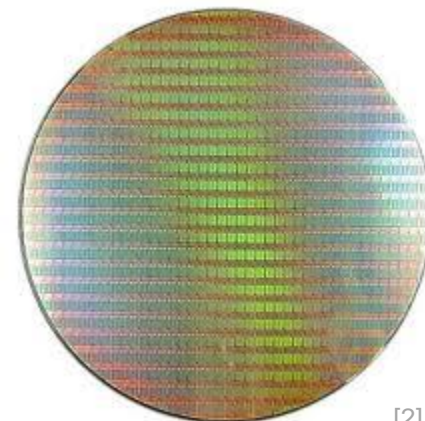
TCAD stands for “**Technology Computer Aided Design**” where a software tool is used to simulate the semiconductor process technology and a device’s electrical, thermal and optical properties

## Why TCAD?

TCAD can boost **productivity** and increase **efficiency** for semiconductor technology development in Foundries, IDMs and even fabless companies. TCAD is like **Virtual Fabrication and Testing** of semiconductors



[1]



[2]



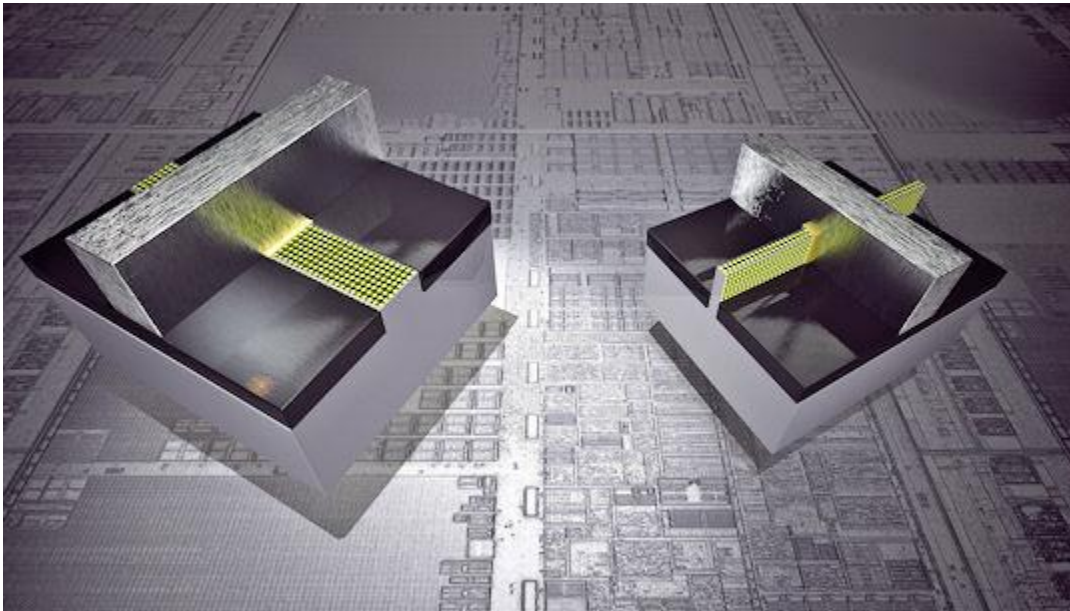
# Why 3D TCAD?

For decades, TCAD has been limited to 2D, because:

- Lack of computing power for the simulator
- Device structures have little variations in the third dimension

Nowadays 3D simulation is increasingly important:

- Pronounced three dimensional effect
- Better understanding of device physics

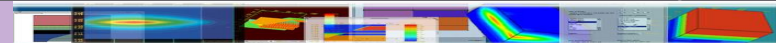


[3]



[4]

Intel's latest 22nm Ivy Bridge processor featuring 3D FINFET



# Contents

## 3D TCAD mesh generation with stacked straight planes

- Example 1: CMOS Image Sensor
- Example 2: CMOS Process Flow
- Example 3: Super Junction LDMOS
- Example 4: Complex Interconnect
- Example 5: FINFET simulated with NEGF
- Example 6: Racetrack LDMOS

## 3D stacked bent planes

- Example 1: Array of silicon pillars
- Example 2: Racetrack LDMOS comparison
- Example 3: 3D diodes breakdown
- Example 4: Vertical DMOS and vertical diode

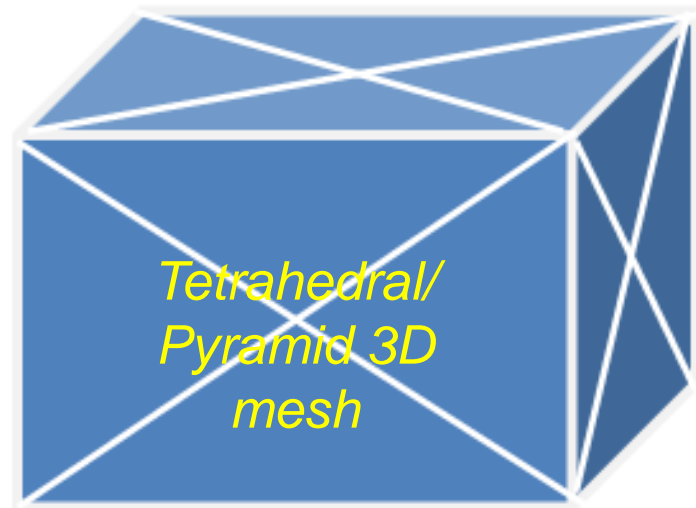
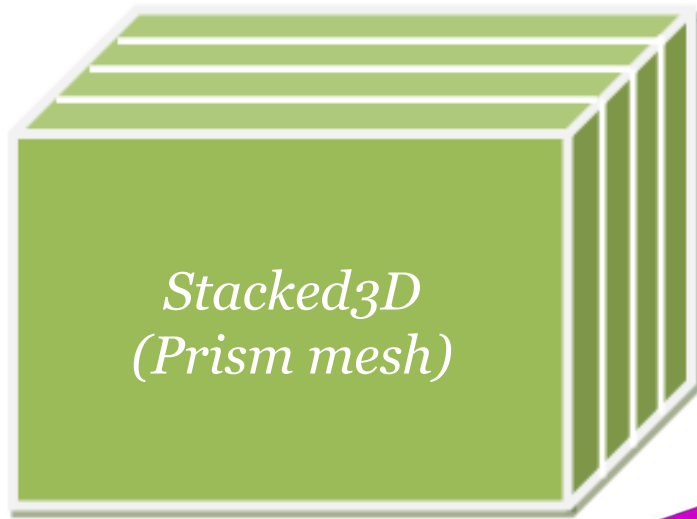
## GPU simulation

- Example 1: FDTD of light propagation and optical intensity
- Example 2: 3D circular LDMOS growth
- Example 3: LIGBT

## Summary



# 3D TCAD Mesh Generation



## Prism Mesh

- ✓ Higher Efficiency
- ✓ Easier to build and control
- ✓ Directly extract 2D planes
- ✓ Better convergence
- ✗ Relatively new

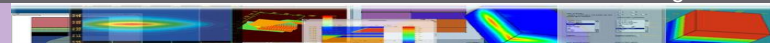
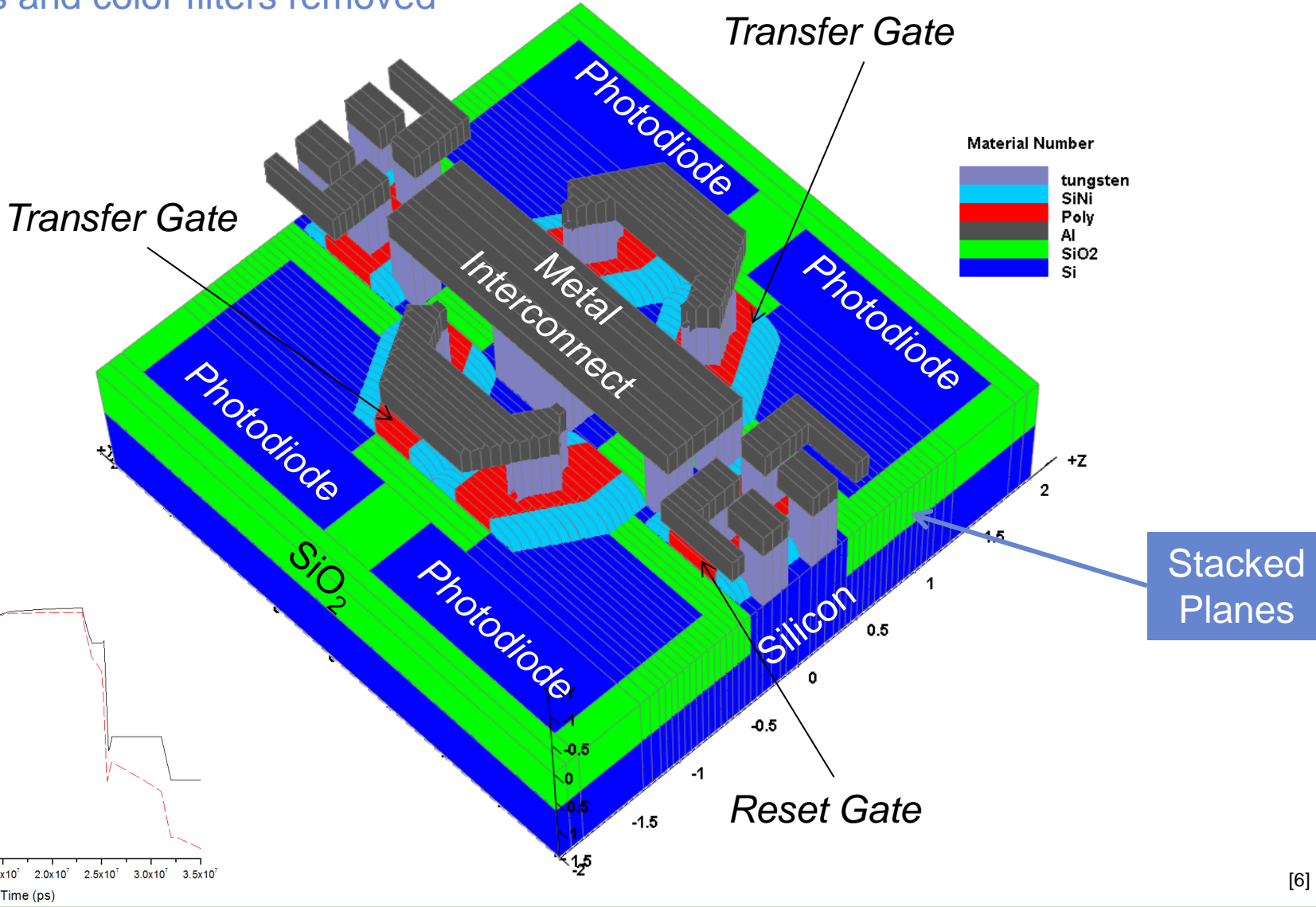
## Tetrahedral Mesh

- ✓ Relatively mature
- ✓ Available from many vendors
- ✗ Less efficient
- ✗ Difficult to control
- ✗ Convergent problems

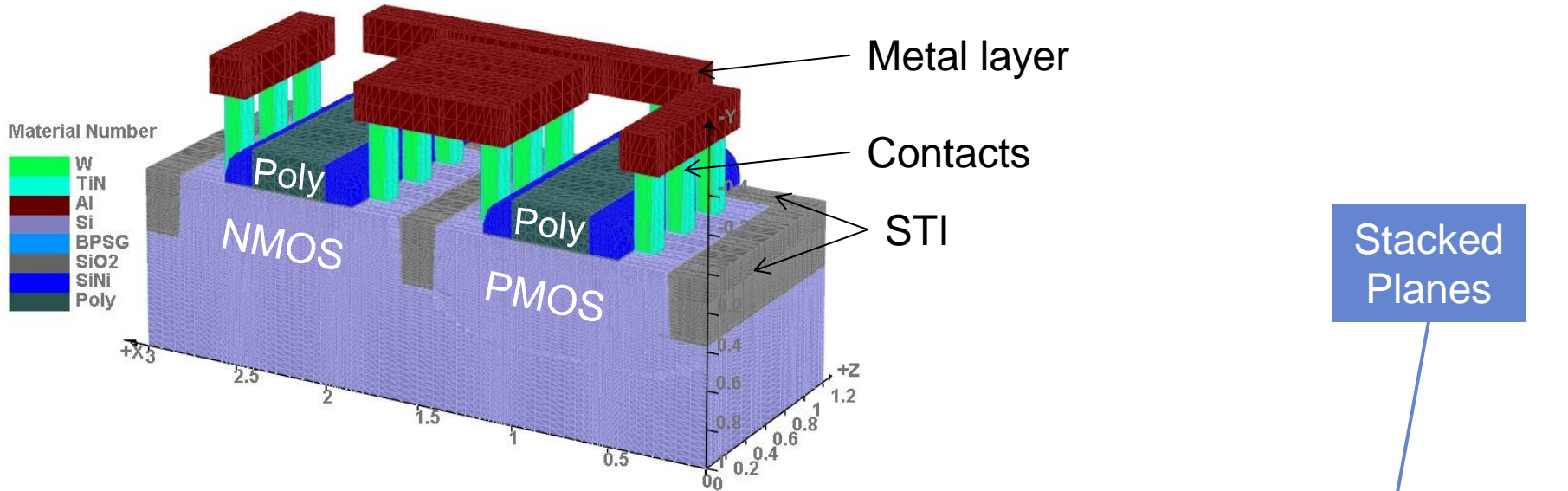


# Example: CMOS Image Sensor

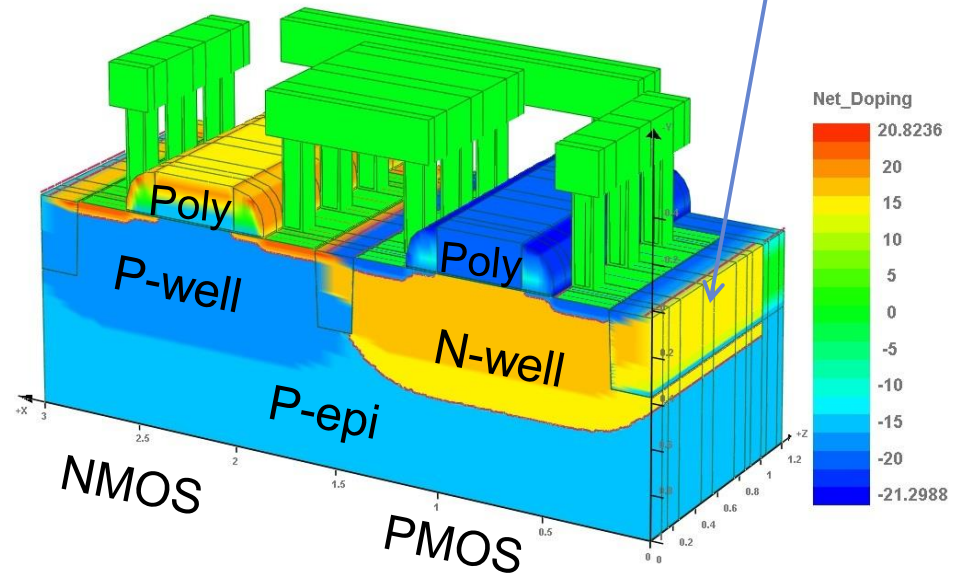
With lens and color filters removed



# Example: CMOS Process Flow

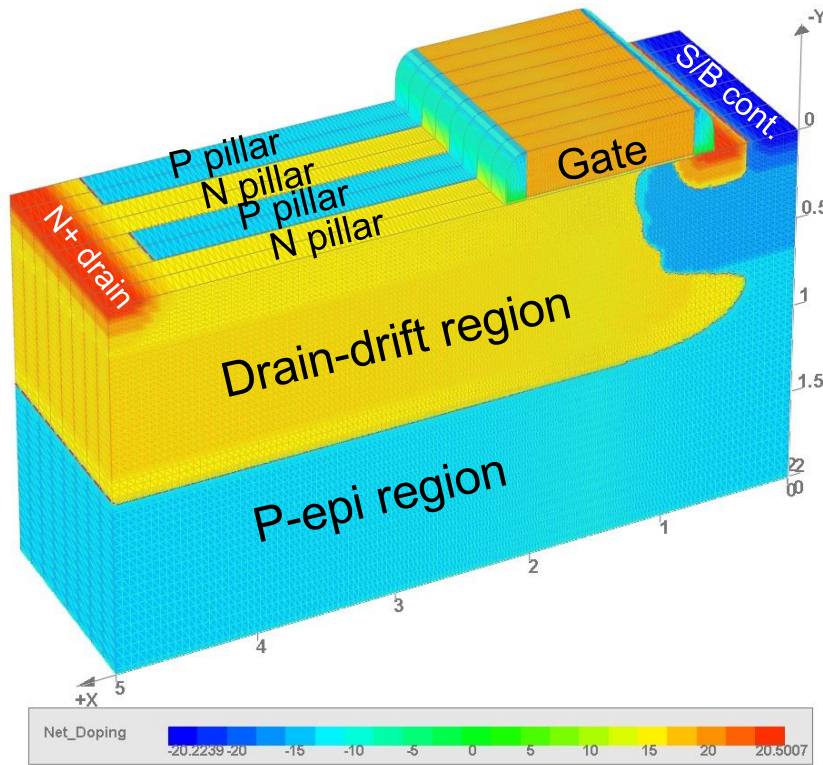


NMOS and PMOS are grown side by side and isolated by STI



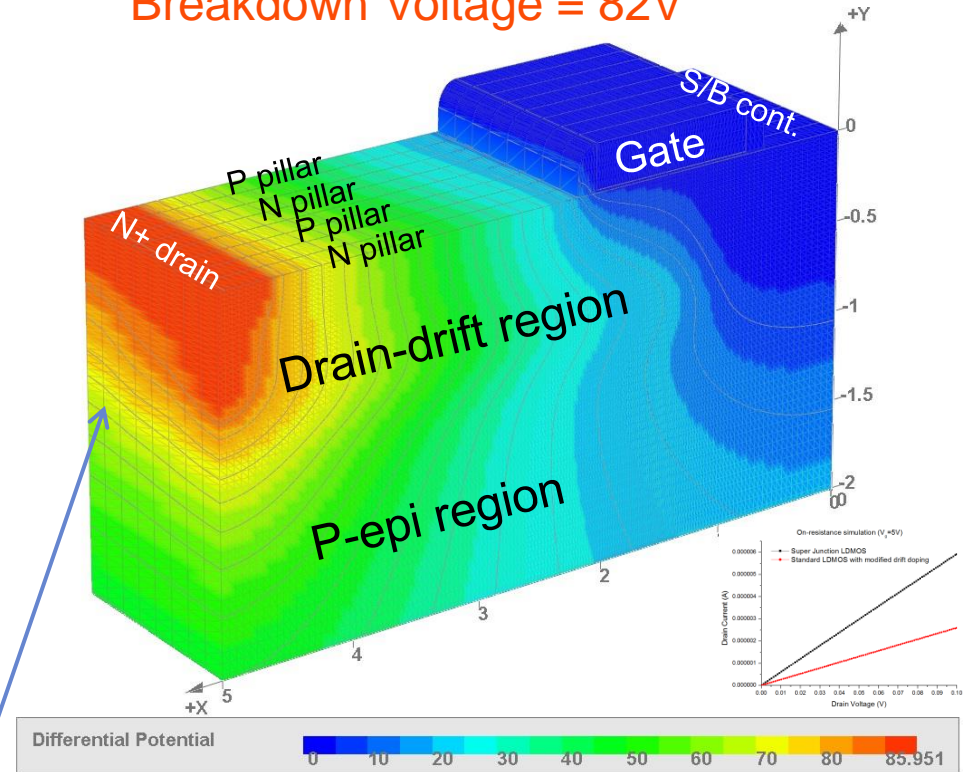
# Example: Super Junction LDMOS

Super Junction LDMOS can achieve lower on-resistance with the same breakdown voltage as conventional LDMOS



Net doping concentration plot

Breakdown Voltage = 82V



Potential plot after breakdown

Stacked  
Planes

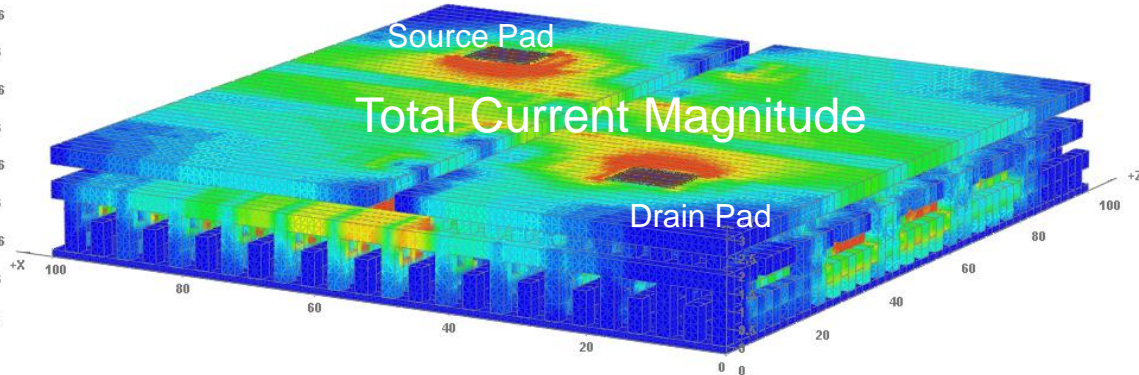
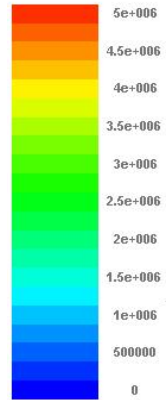


# Example: Complex Interconnect

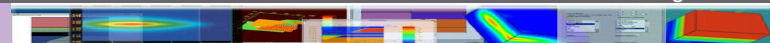
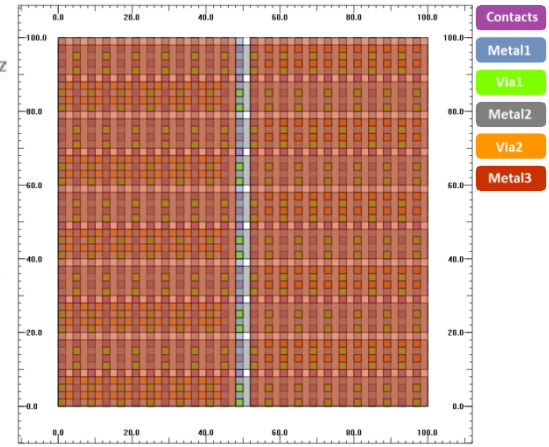
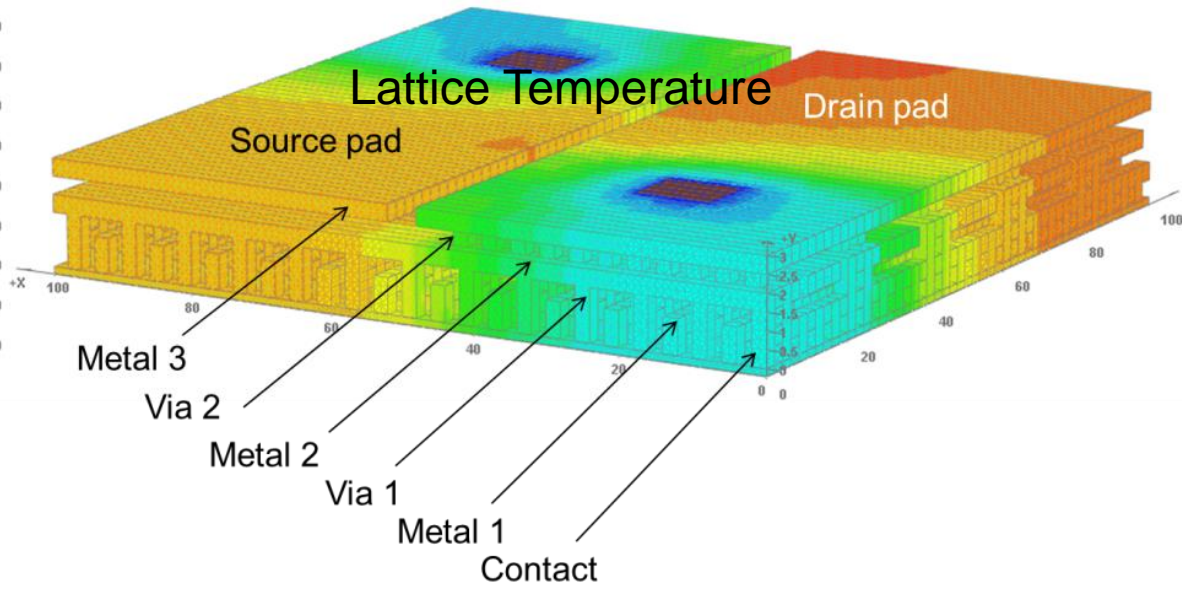
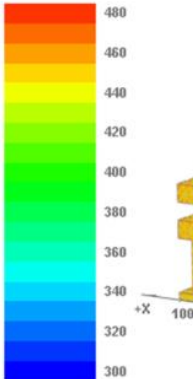
Interconnect current magnitude and lattice temperature distribution at high current bias

Total Mesh points: 110,000  
Total stacked planes: 100

Total Curr. Mag (A/cm<sup>2</sup>)

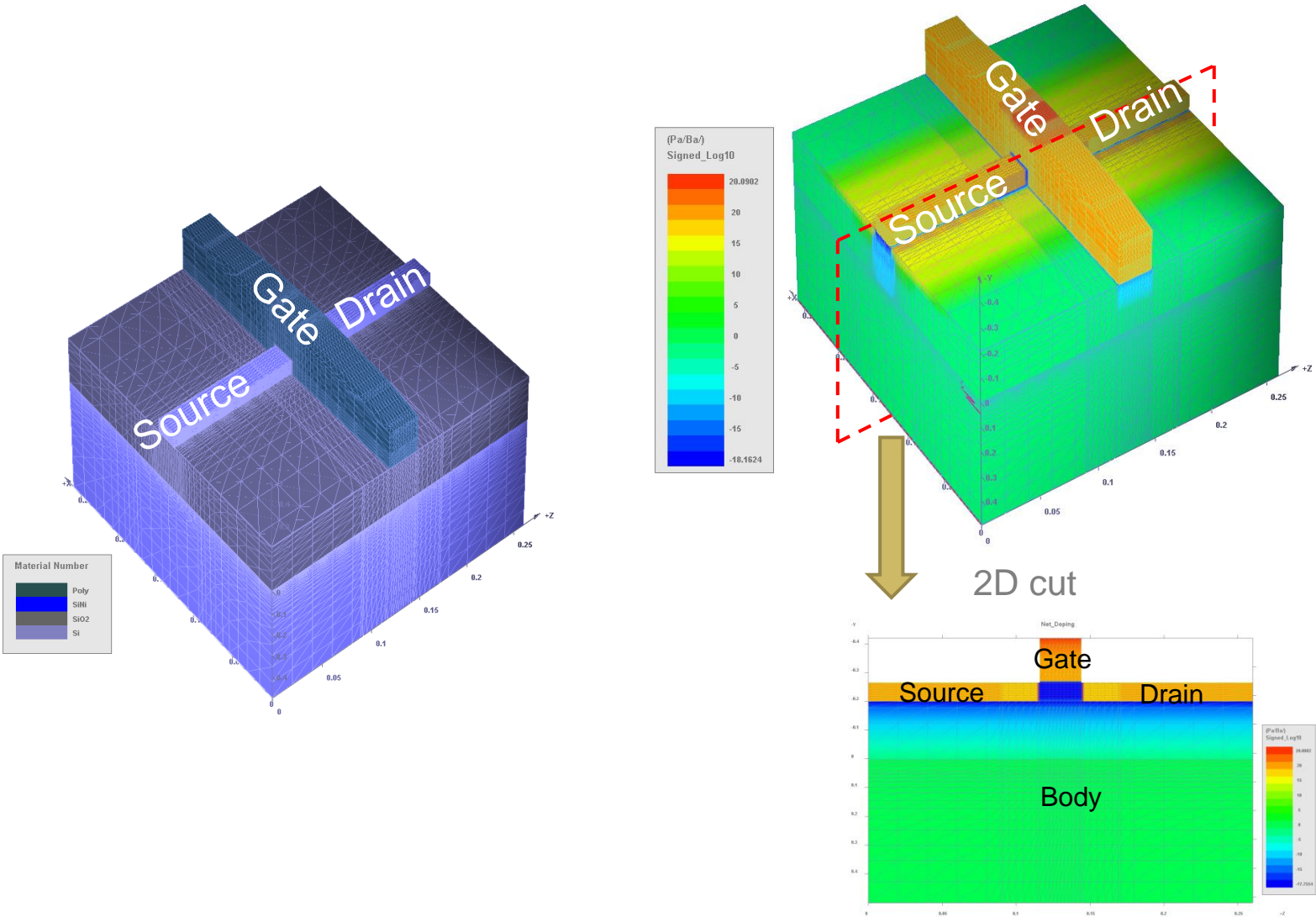


Lattice Temperature (K)



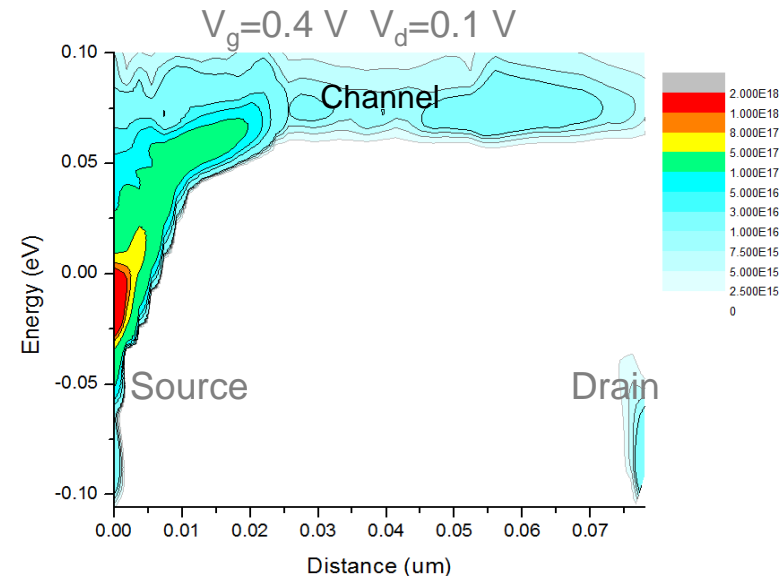
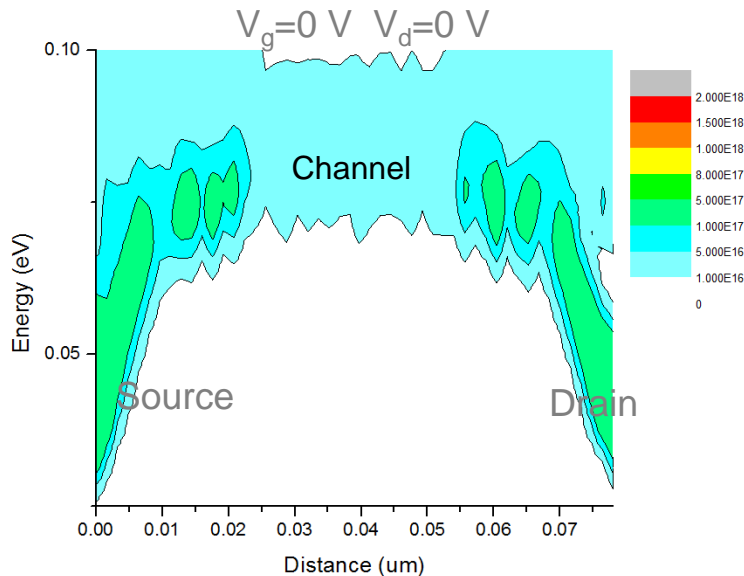
# Example: FINFET with NEGF

A simple FINFET is simulated with Non-Equilibrium Green's Function (NEGF)

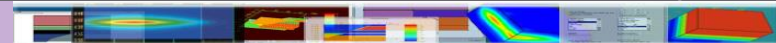


# Example: Simple FINFET with NEGF

- The device is divided into classical drift-diffusion (DD) region (mainly in vicinity of source/drain contacts) and quantum ballistic transport (QBT) region in the channel
- NEGF (Non-Equilibrium Green's Function) model is employed in QBT region
- Poisson's equation solver is used in both DD and QBT regions



Electron density of  $val=1$   $sub=1$  along the channel. As  $V_d$  increases, more electrons will be injected from source to drain by ballistic transport.





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## GPU simulation

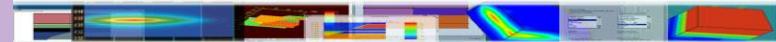
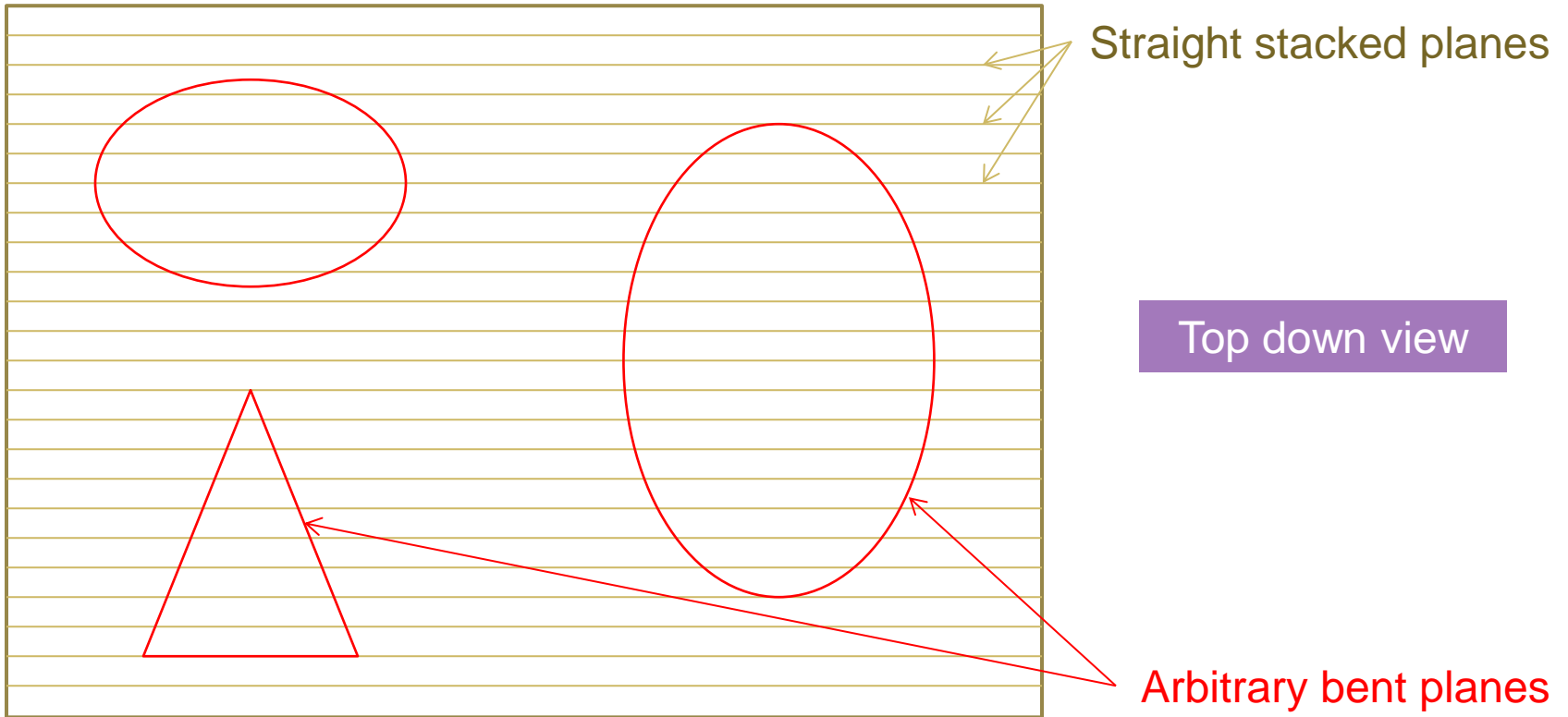
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## Summary



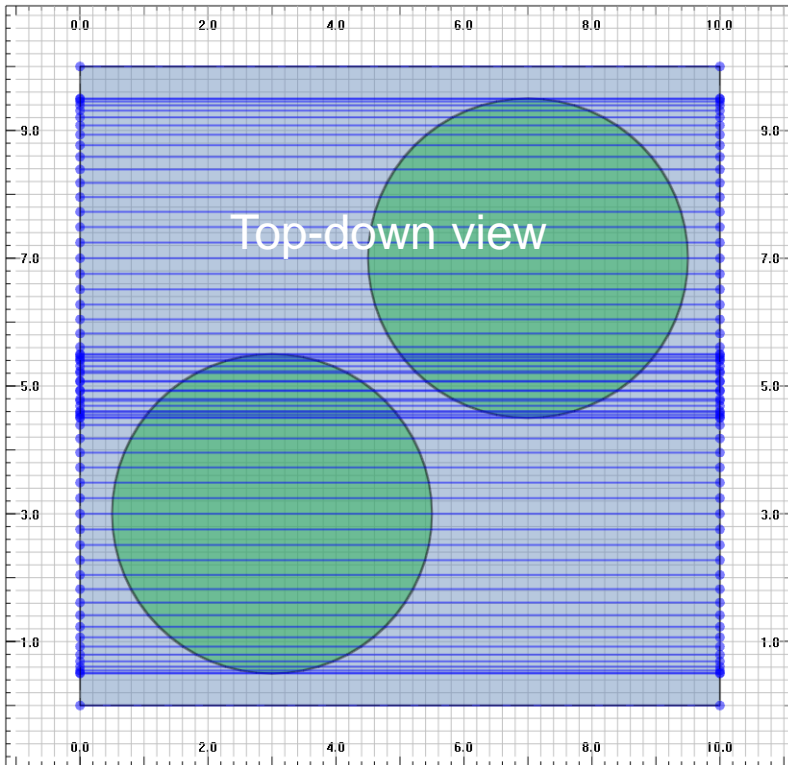
# Bent Planes

While straight stacking planes are good at handling rectangular shaped structures, they can be inefficient for curvatures. For arbitrary and curved structures, a novel method is to apply a new kind of planes called bent planes inserted between straight planes. These bent planes greatly optimize the mesh design in the Z direction

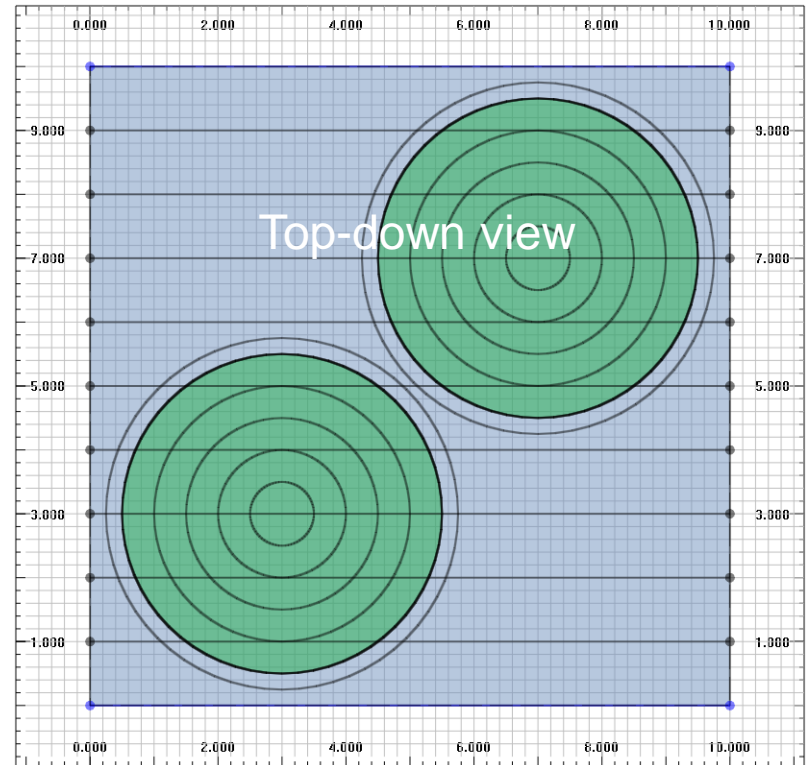


# Bent Planes

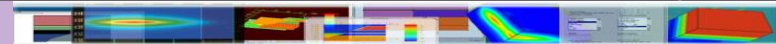
Straight planes + bent planes solution can help reduce the total mesh and avoid the unnecessarily dense mesh locations in the straight planes only method



With straight planes only (75)  
Mesh size: 33000

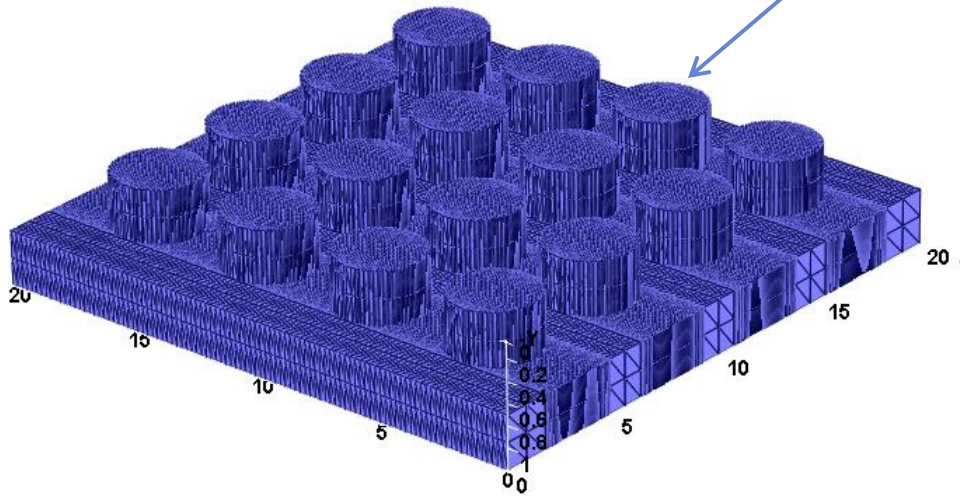


Straight planes (9) + bent planes (12)  
Mesh size: 4800



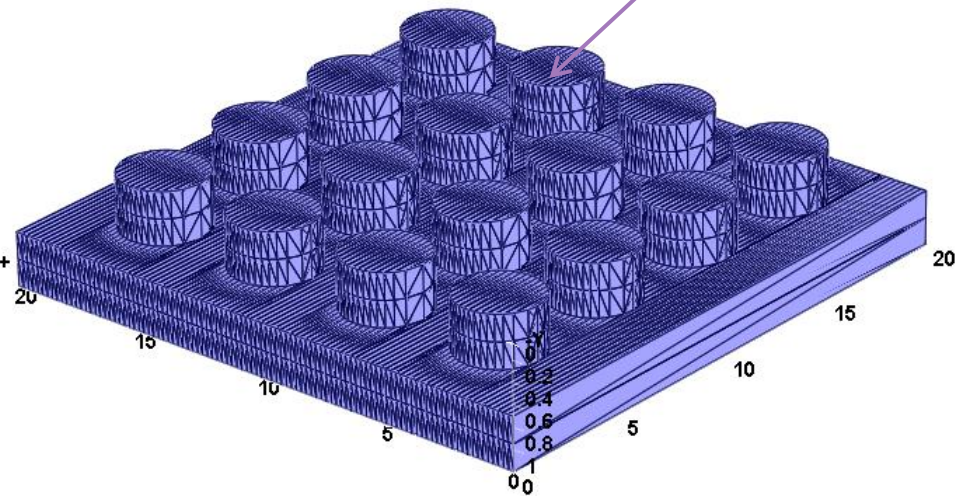
# Example: Array of Silicon Pillars

Stacked Straight Planes



- Total Mesh Count: 52682
- Straight planes: 134
- Process Simulation time: 50 minutes

Stacked Bent Planes



- Total Mesh Count: 4958
- Planes: 2 straight+ 16 bent planes
- Process Simulation time: 2 minutes

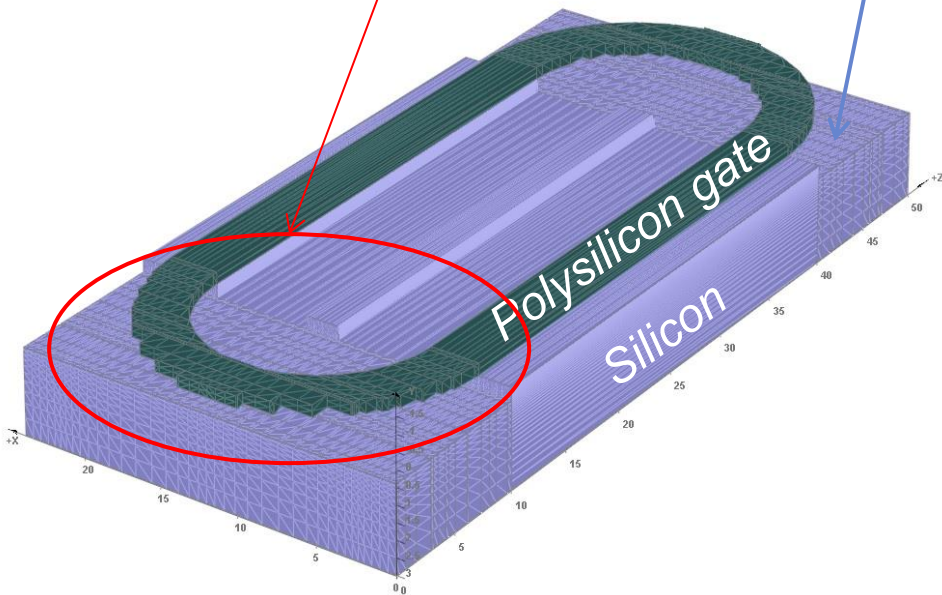




# Example: Racetrack LDMOS

Not smooth

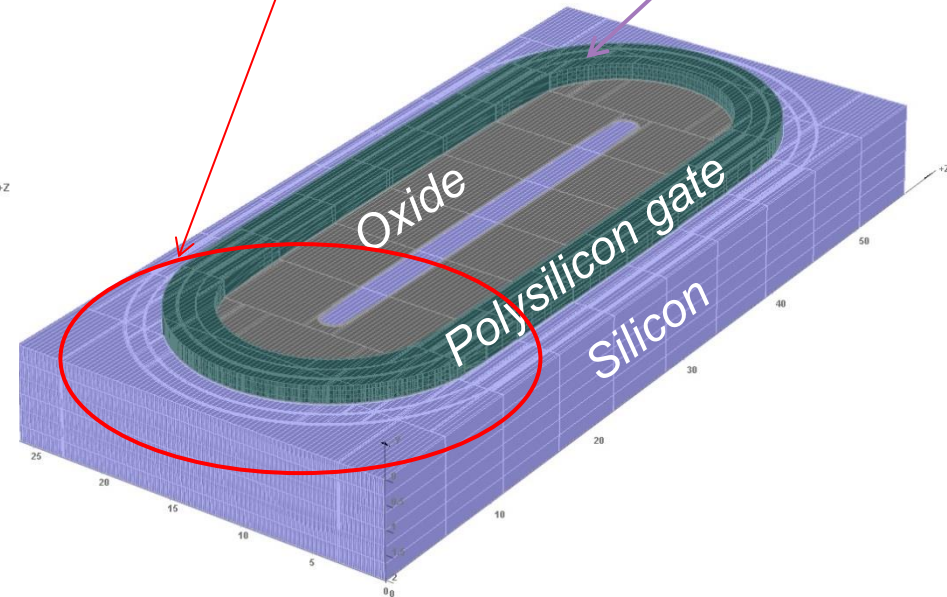
Stacked Straight  
Planes



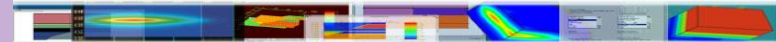
Structure with straight stacked planes only  
(with oxide and metal layers removed)

Very smooth

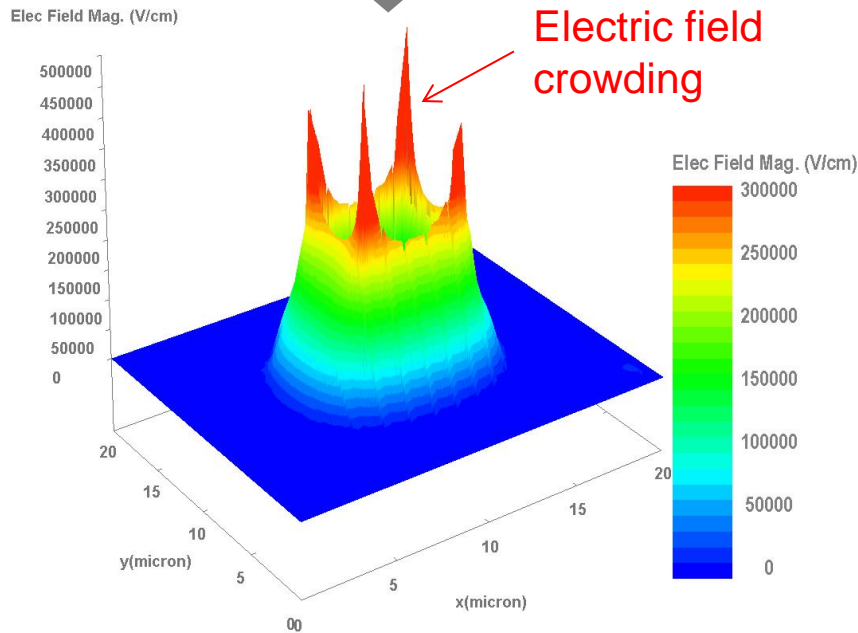
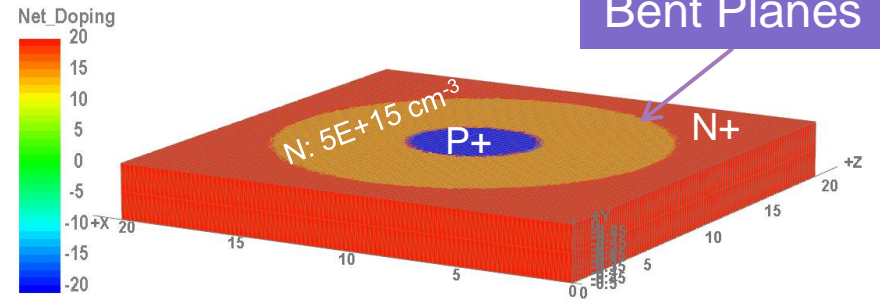
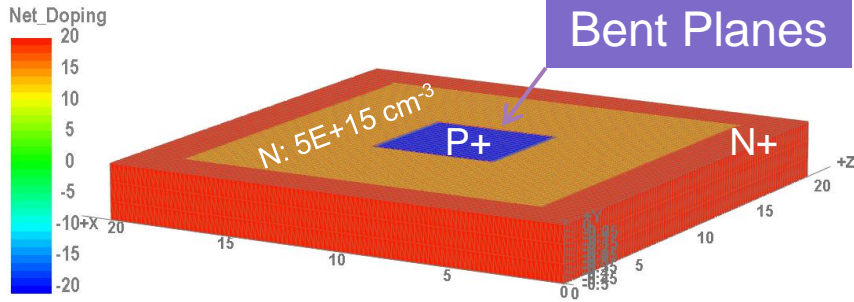
Stacked  
Bent Planes



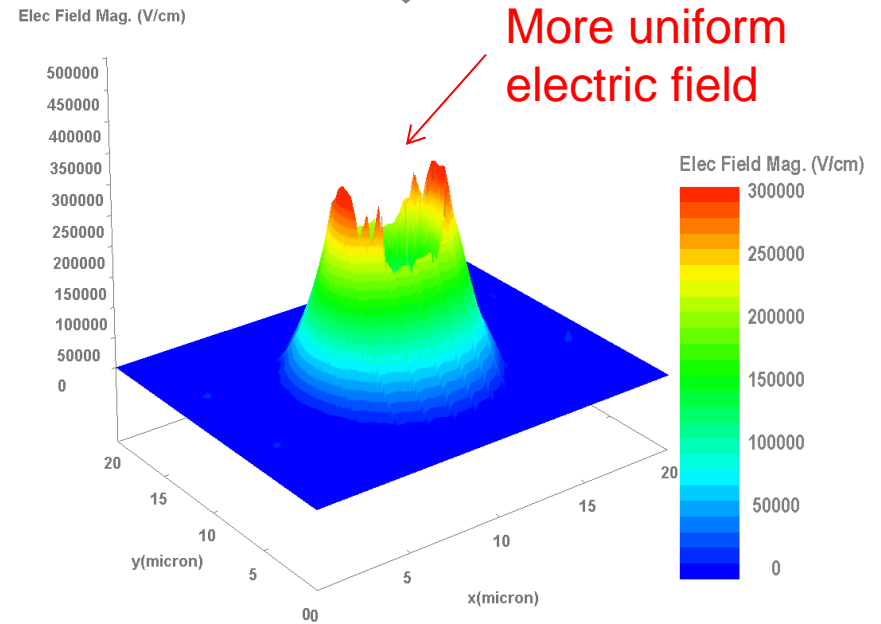
Structure with straight and bent planes  
(with metal layers removed)



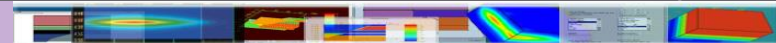
# Example: 3D Diodes Breakdown



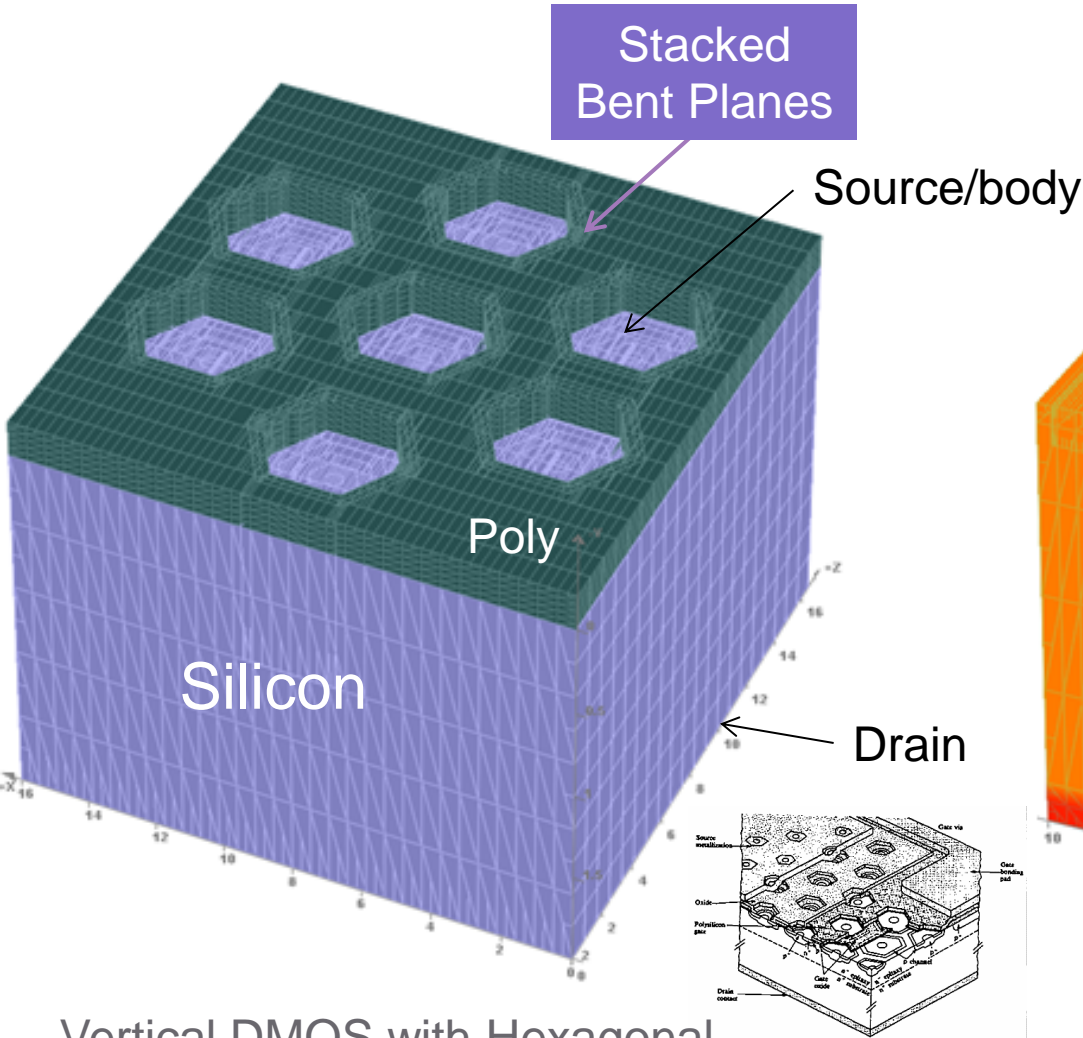
Breakdown Voltage= 50V



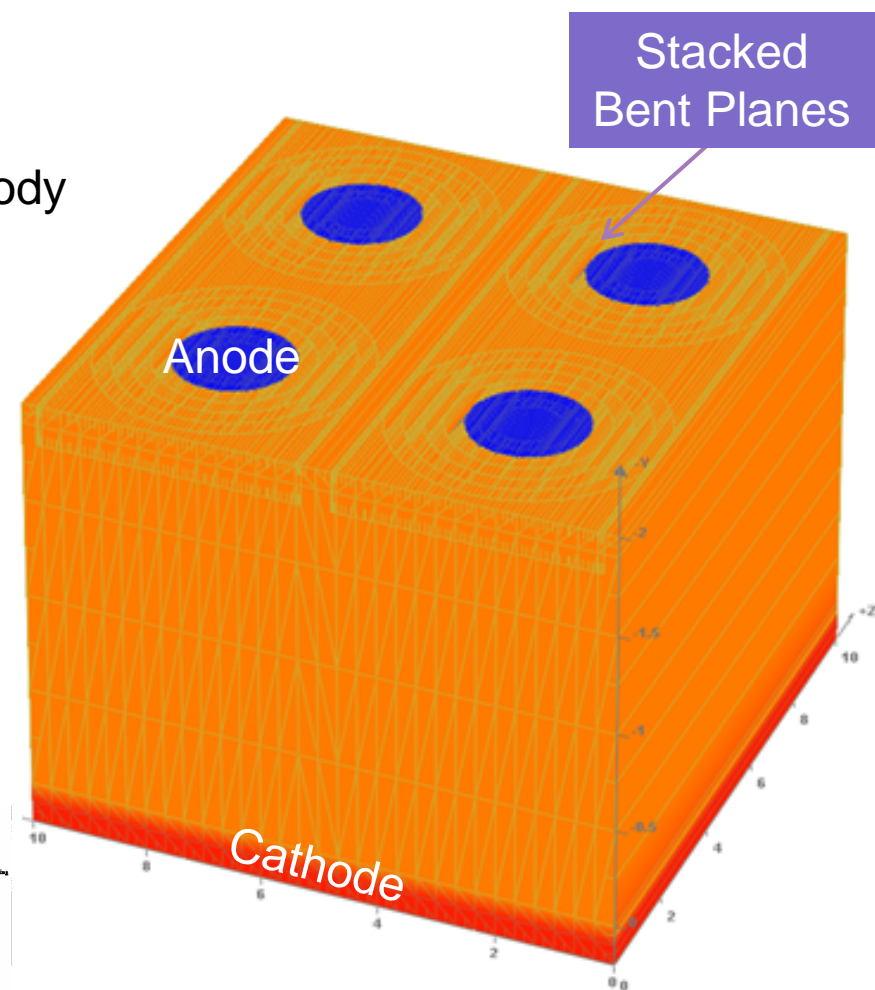
Breakdown Voltage= 67V



# Example: Vertical DMOS and Diode



Vertical DMOS with Hexagonal shaped gates



Vertical diodes structure

<http://www.irf.com/technical-info/guide/device.html>



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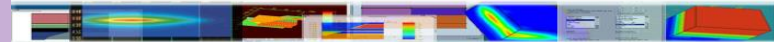
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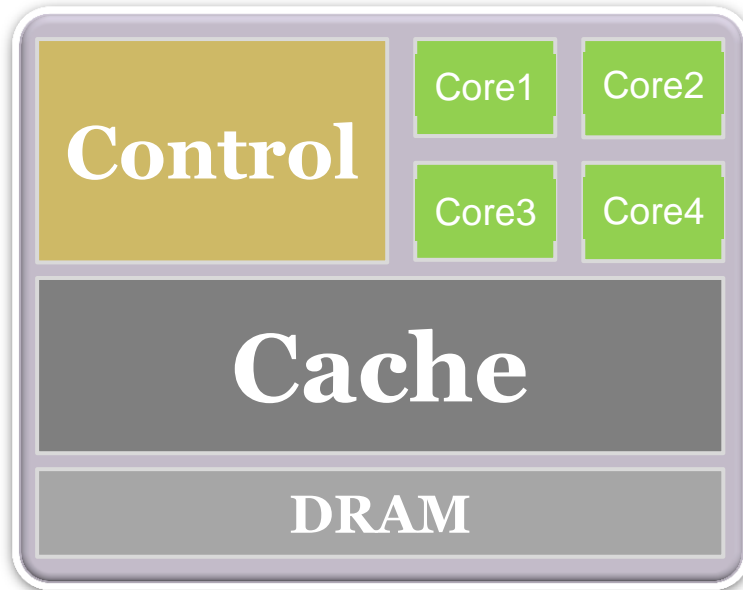
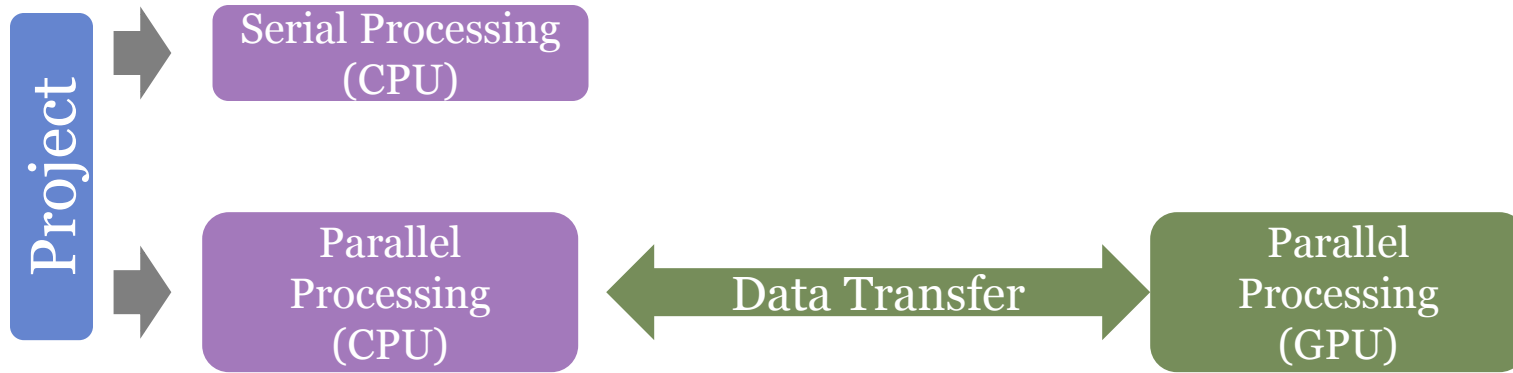
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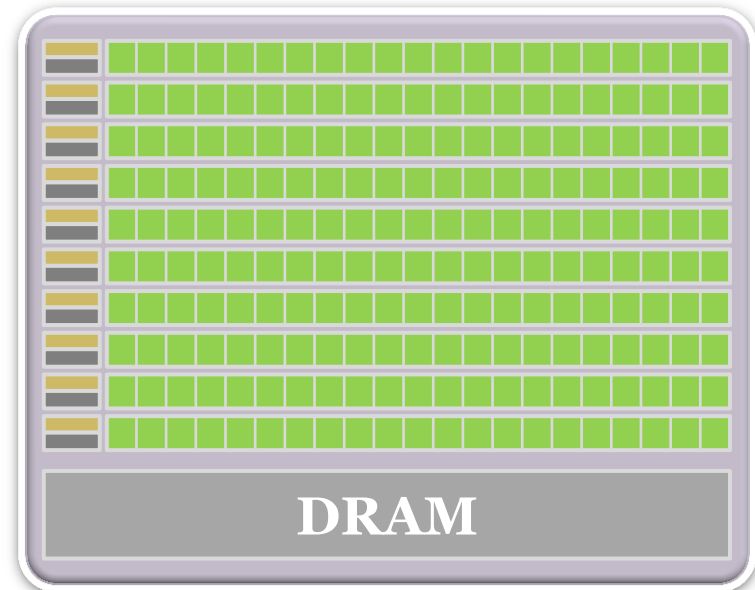
## Summary



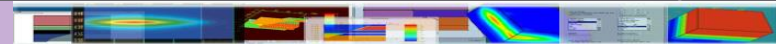
# GPU Simulation



Simplified CPU Architecture

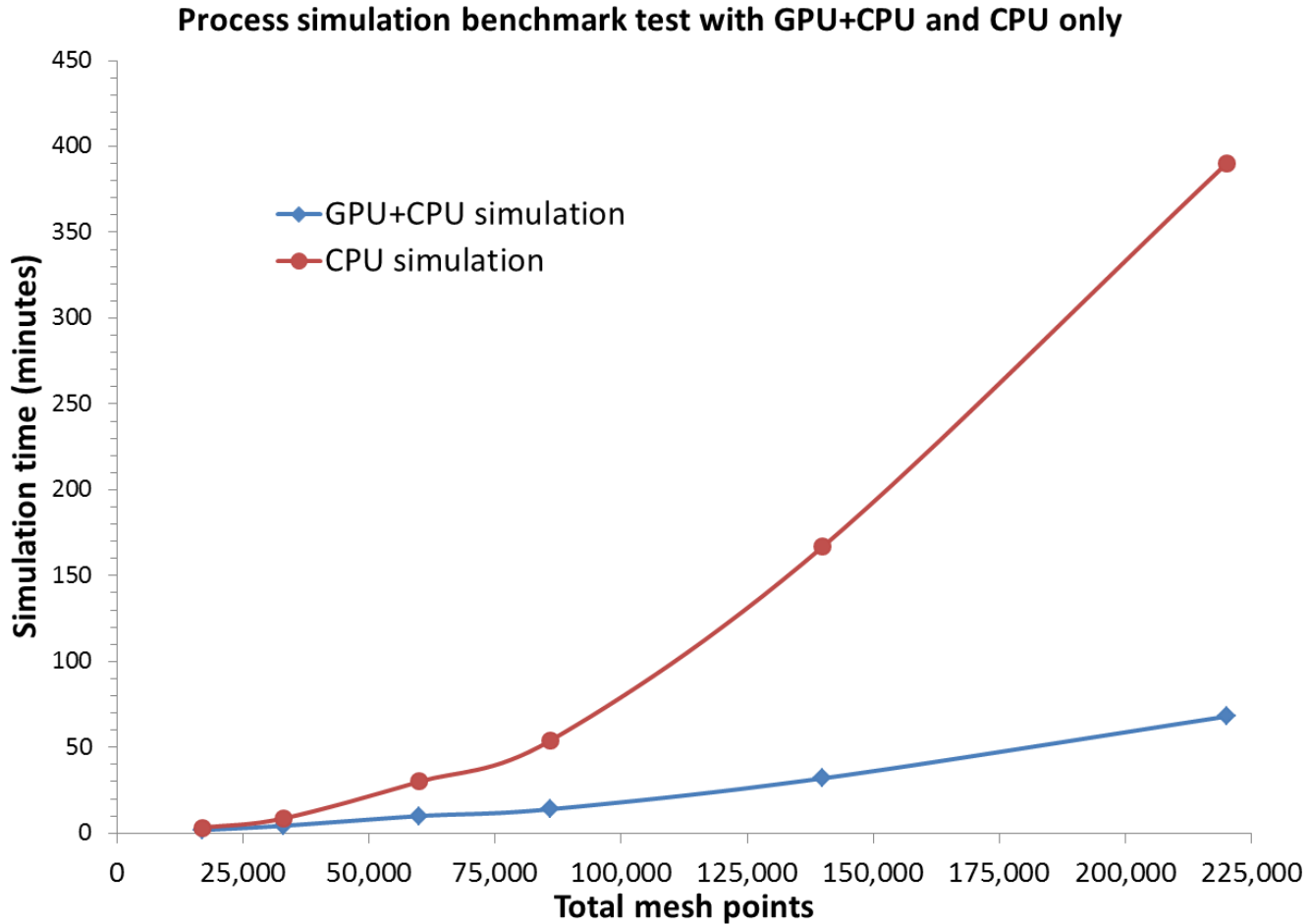


Simplified GPU Architecture

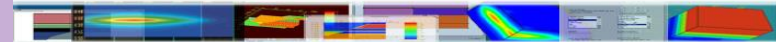


# GPU Simulation Benchmark

GPU (Graphic Processing Unit) simulation enables large scale parallels simulation to greatly reduce simulation time

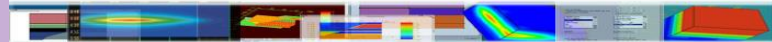


Intel core i7 3770 with 32 G memory and 64bit Windows 7 OS. GPU: NVidia Geforce GTX 690



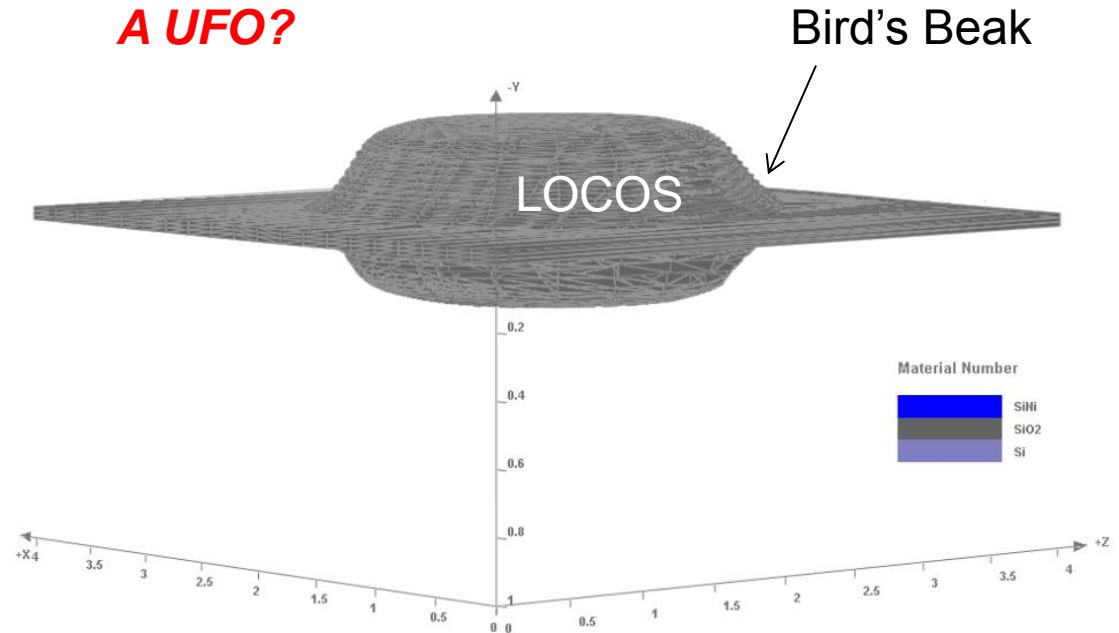
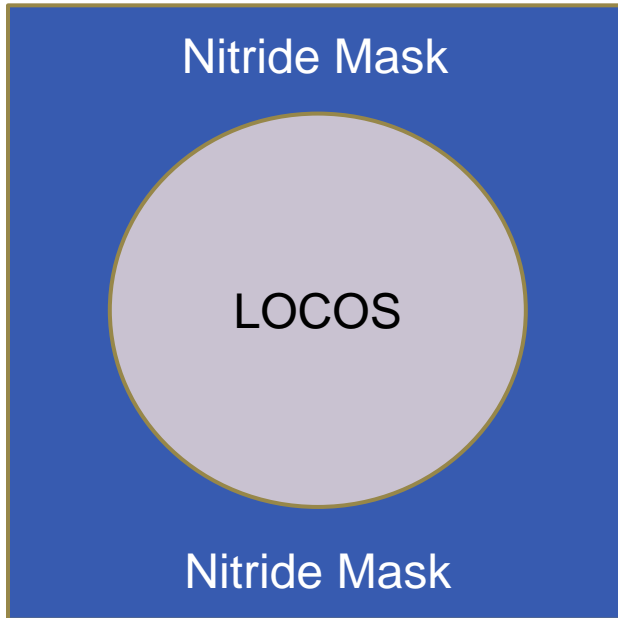
# GPU Simulation:

FDTD (Finite-difference time-domain) simulation of light propagation and optical intensity from top of a lens

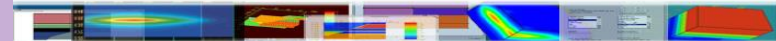


# Example: 3D Circular LOCOS Growth

LOCOS: Local Oxidation of Silicon, simulated with GPU



Oxidation and diffusion are the most time consuming steps in a semiconductor process simulation. Fortunately, it is possible to make the simulation job done in parallel. GPU simulation of oxidation and diffusion greatly reduces the total simulation time

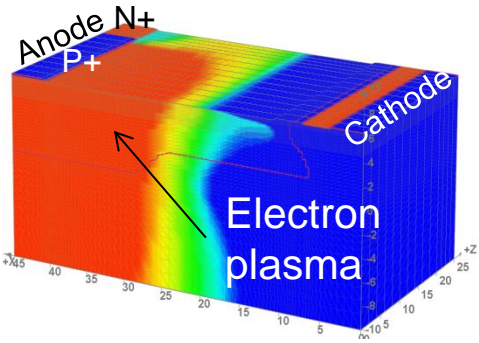




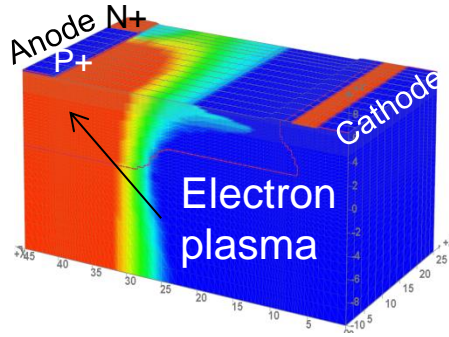
# Example: LIGBT Switch-off Transient

Transient simulation of a segmented anode Lateral Insulated Gate Bipolar Transistor (LIGBT) with GPU

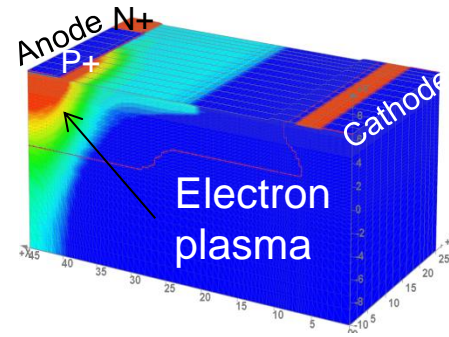
Electron plasma diminishing in the silicon overtime



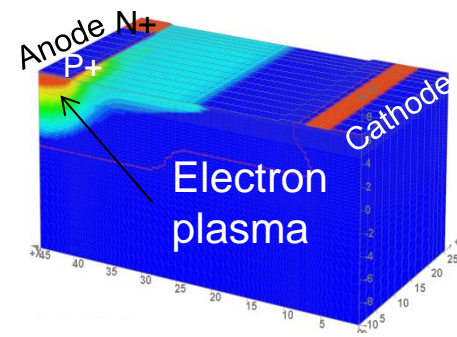
10 ns



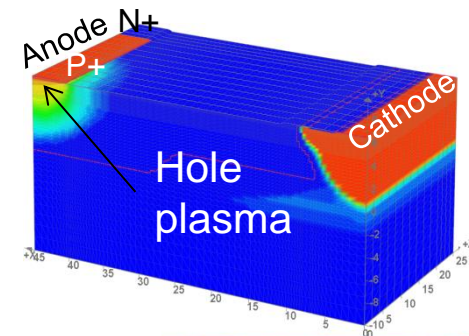
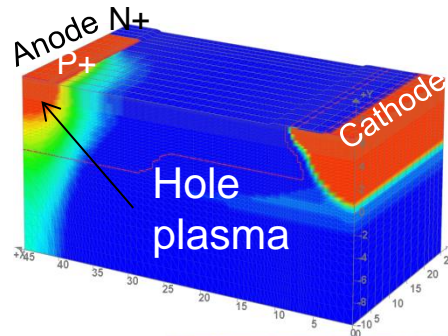
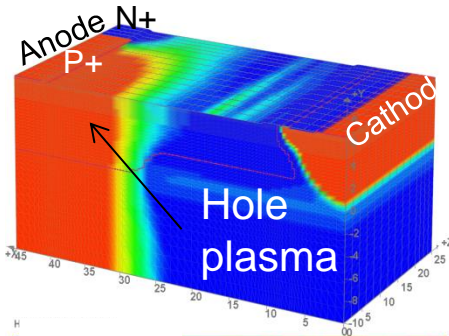
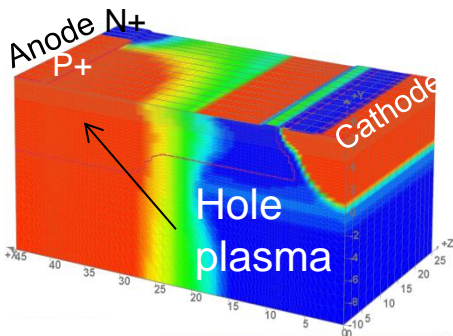
35 ns



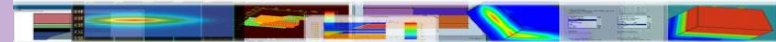
110 ns



125 ns



Hole plasma diminishing in the silicon overtime



# Summary

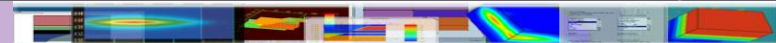
## Practical new approaches for 3D TCAD simulation:

- ✓ Prism mesh instead of conventional pyramid mesh for less convergent issues and more efficient mesh generation
- ✓ Bent planes are created for curvatures and arbitrary shapes in the Z direction
- ✓ GPU simulation can dramatically reduce simulation time

\* CPU: i7-3770, GPU: NVidia Geforce GTX 690, Memory: 32 G

Devices	Mesh size	Process simulation time (GPU)	Device simulation time (GPU)
3D E-field	35,000	20 minutes	1.1 hours
LIGBT	167,000	2 hours	35 hours
Super Junction LDMOS	177,000	4.25 hours	55 hours

*Thank You*



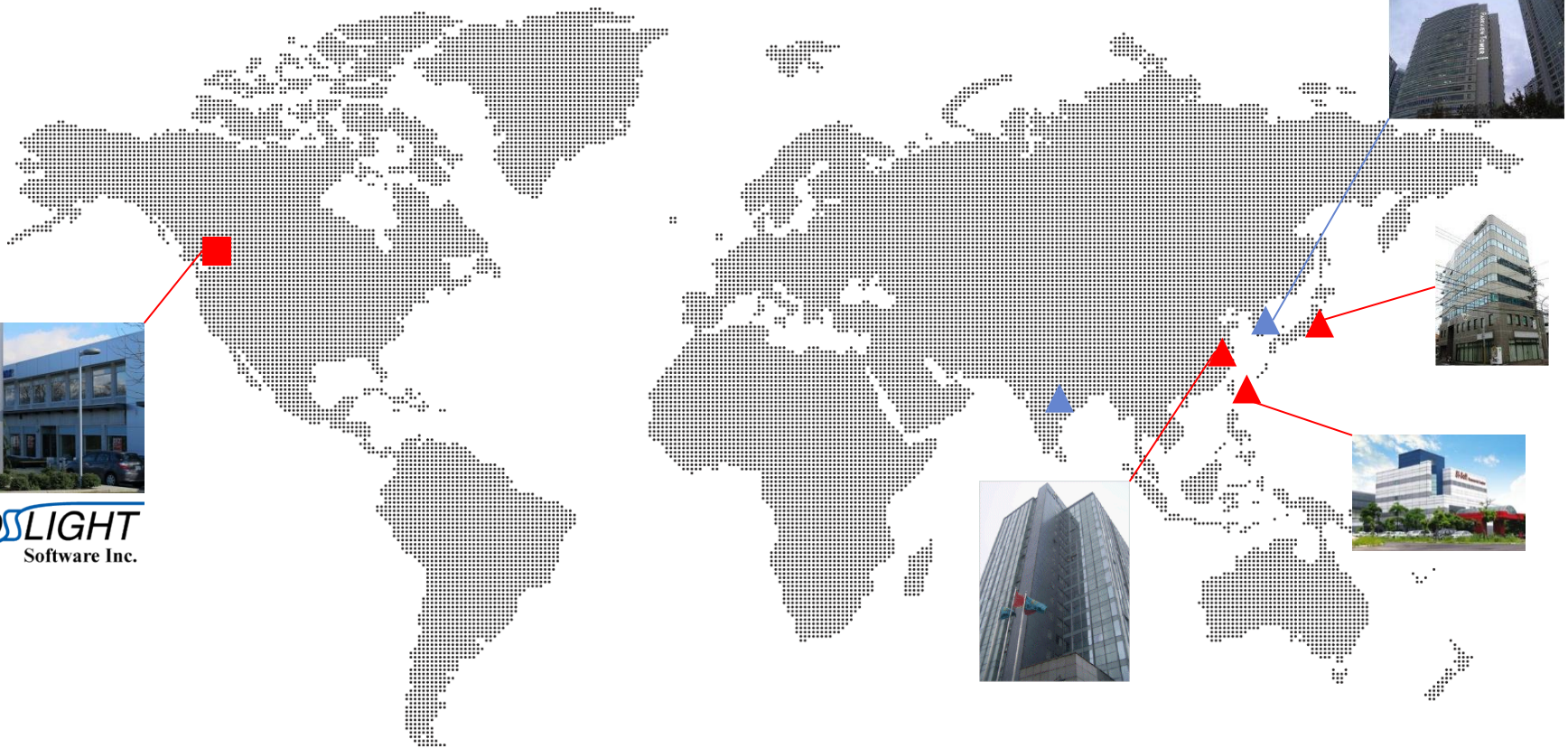
# About Crosslight

A Canadian company with **20** years of history

The world's **first** commercial TCAD for laser diode

The world's **No.1** provider of optics and photonics TCAD

The world's **most advanced** stacked planes 3D TCAD



**CROSSLIGHT**  
Software Inc.



# Reference

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