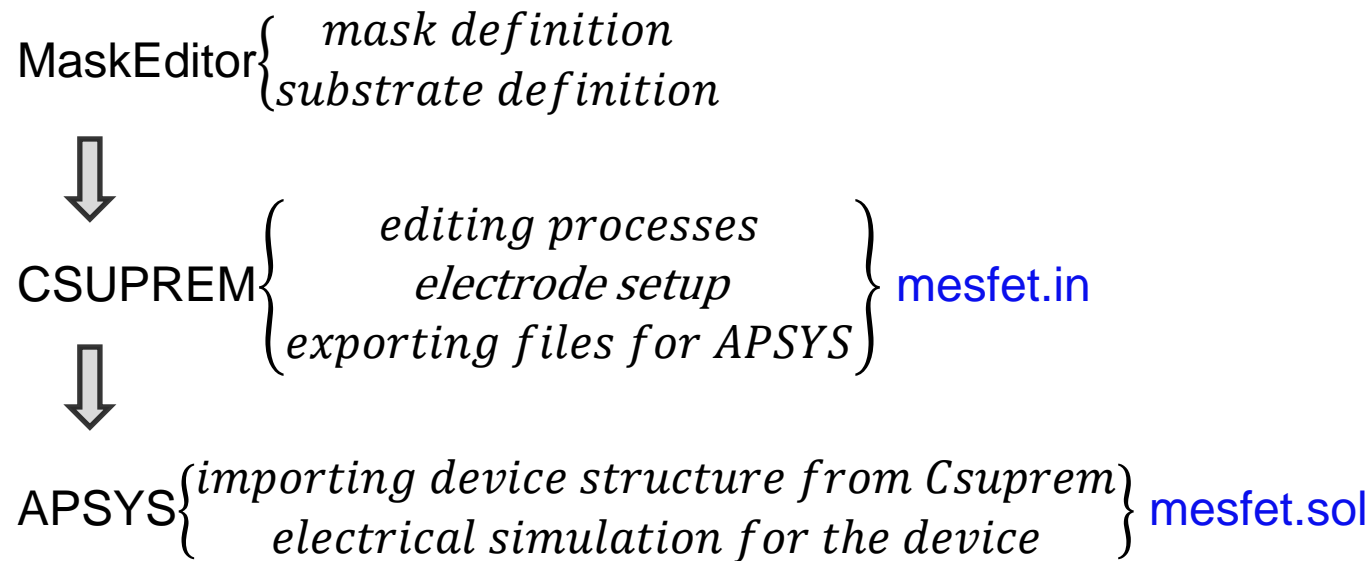


# 3D Simulation of SiC MESFET

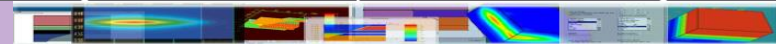
# Introduction to Simulation Flow

3D simulation of a **channel-recessed** SiC MESFET is carried out by *MaskEditor*, *CSUPREM* and *APSYS*.

**File structure in this simulation:**



**Reference structure:** *C.L.Zhu et al. Solid-State Electronics 51 (2007) 343-346*

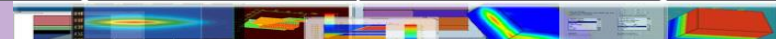
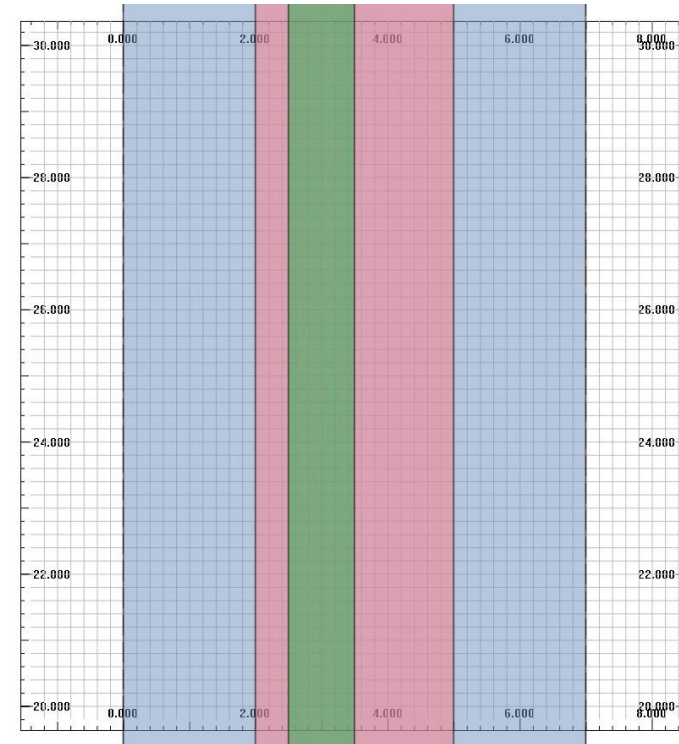


# 3D Process Simulation by MaskEditor

## MESFET mask patterns defined in **MaskEditor**:

- Gray mask is the scope of substrate
- Pink mask is used to remove cap layer
- Green mask is used to generate metal-gate

No.	Label	Color	Purpose	Polarity	Bend
<input checked="" type="checkbox"/> 1	semi_sub	Blue	general	n <input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/> 2	sic_etch	Pink	general	n <input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/> 3	Nickel_etch	Green	general	p <input type="checkbox"/>	<input type="checkbox"/>



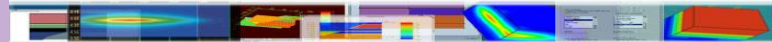
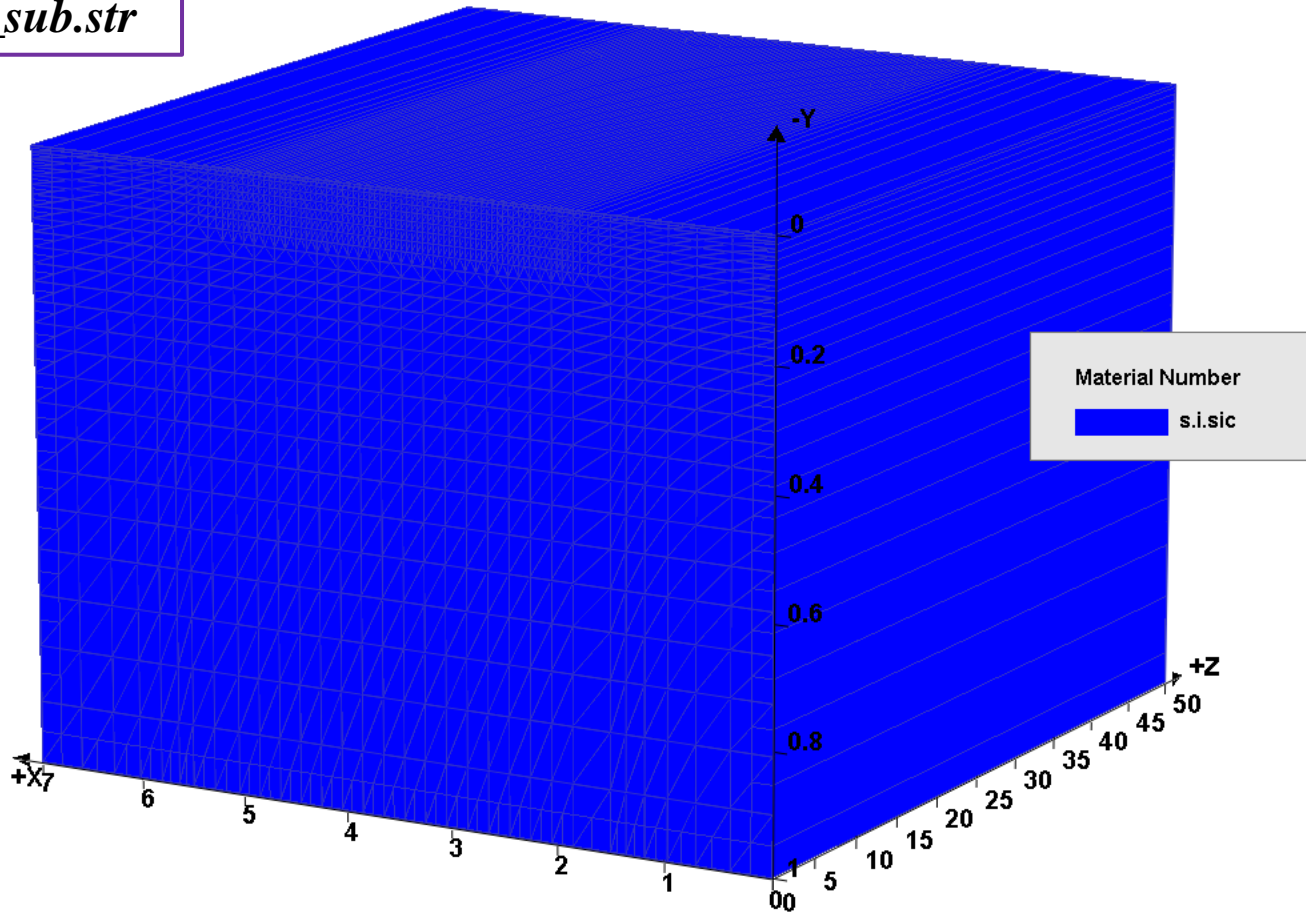
# 3D Process Simulation by CSUPREM

## Simplified processes Step 1: S.I.SiC Substrate

*Run mesfet.in:*

*init*

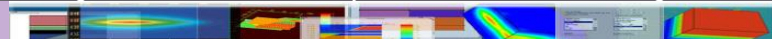
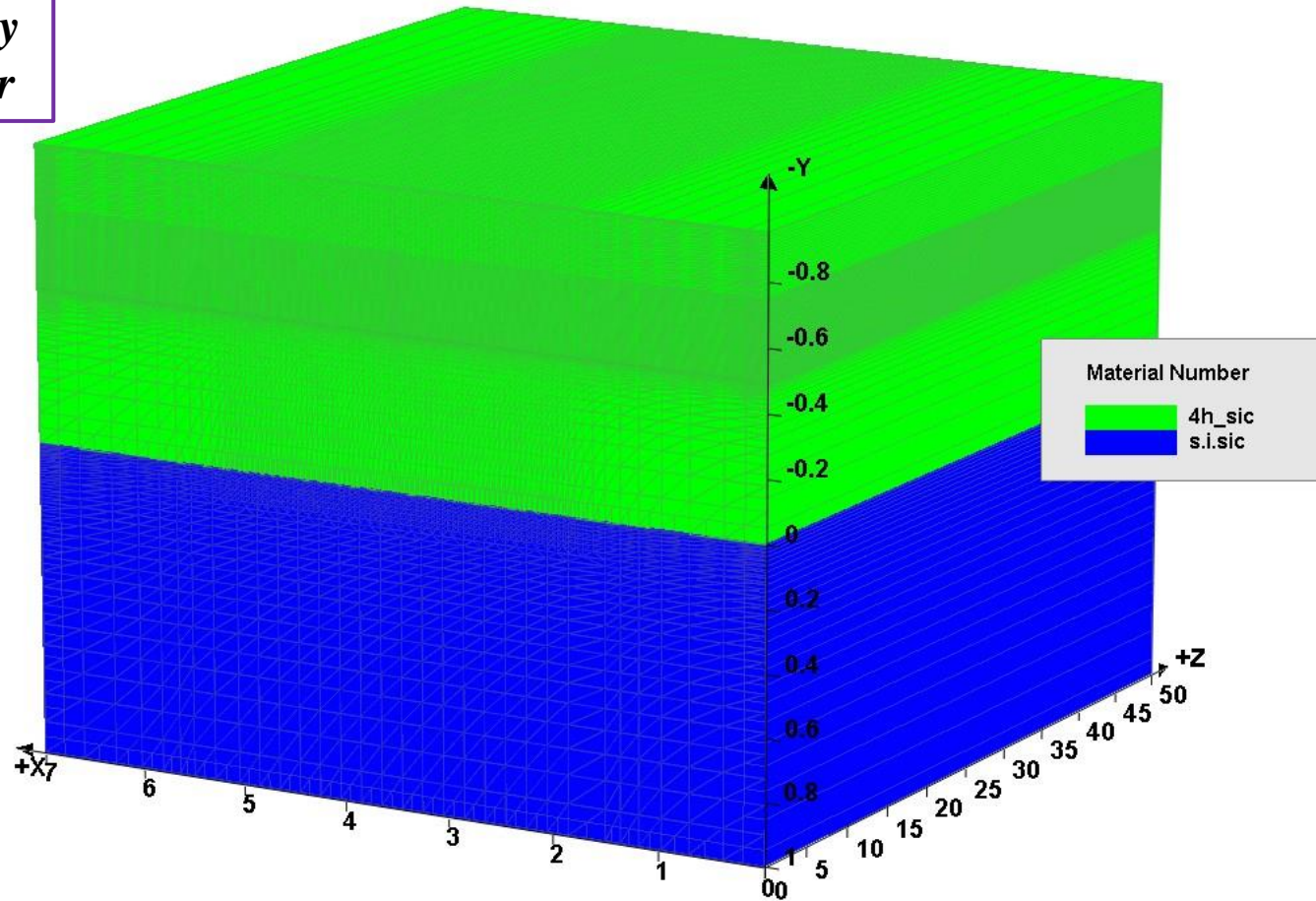
*struct outf=01\_semi\_inlu\_sub.str*



# 3D Process Simulation by CSUPREM

## Step 2: 4H-SiC epitaxy

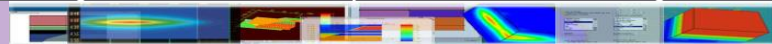
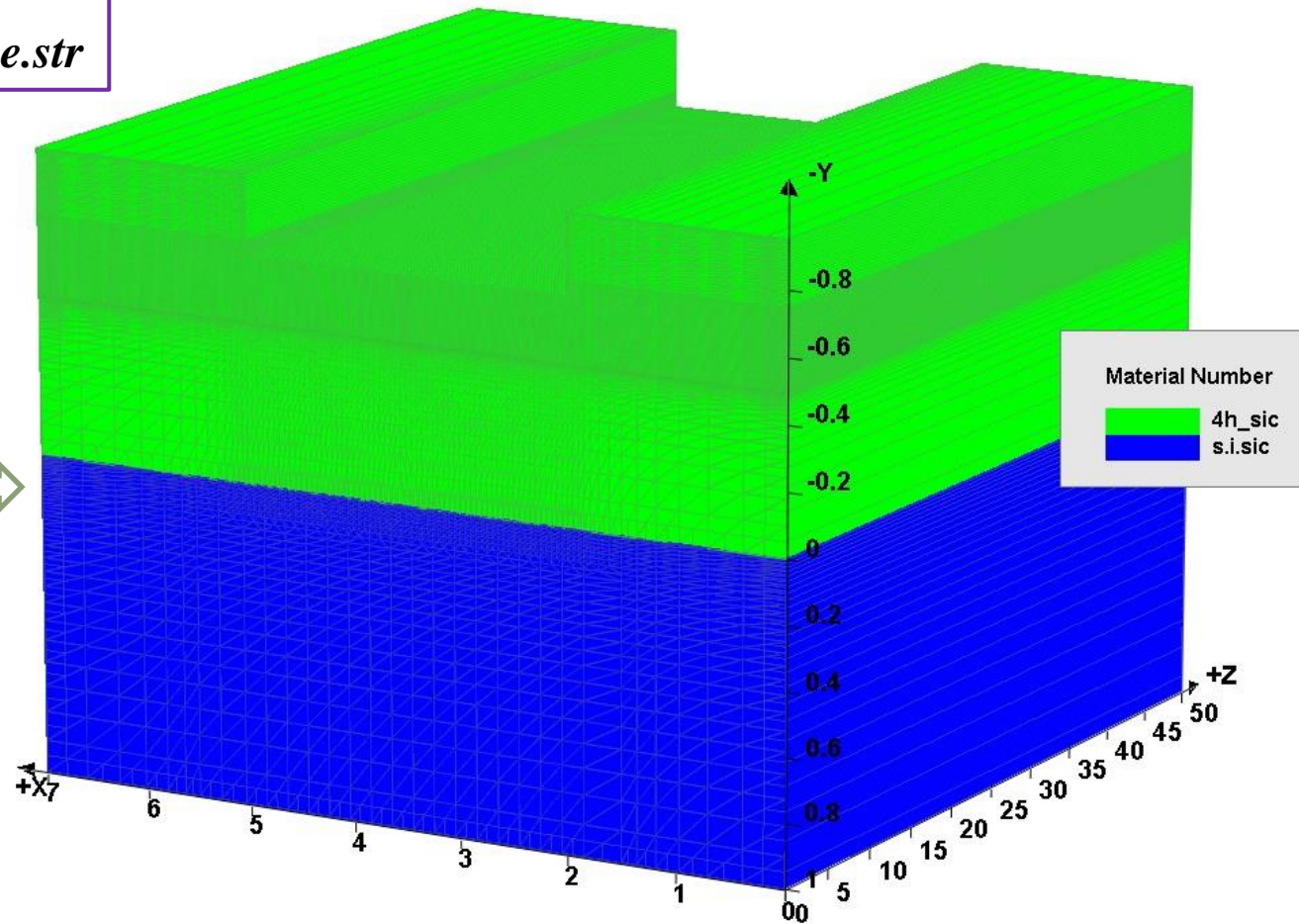
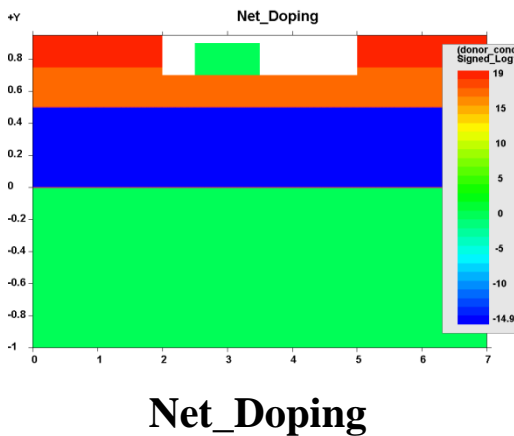
```
include file=mesfet1.msk  
deposit 4h_sic p-buffer  
deposit 4h_sic ni.impurity  
struct outf=02_epitaxy.str
```



# 3D Process Simulation by CSUPREM

## Step 3: dry etch 4H-SiC

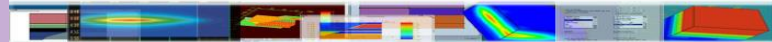
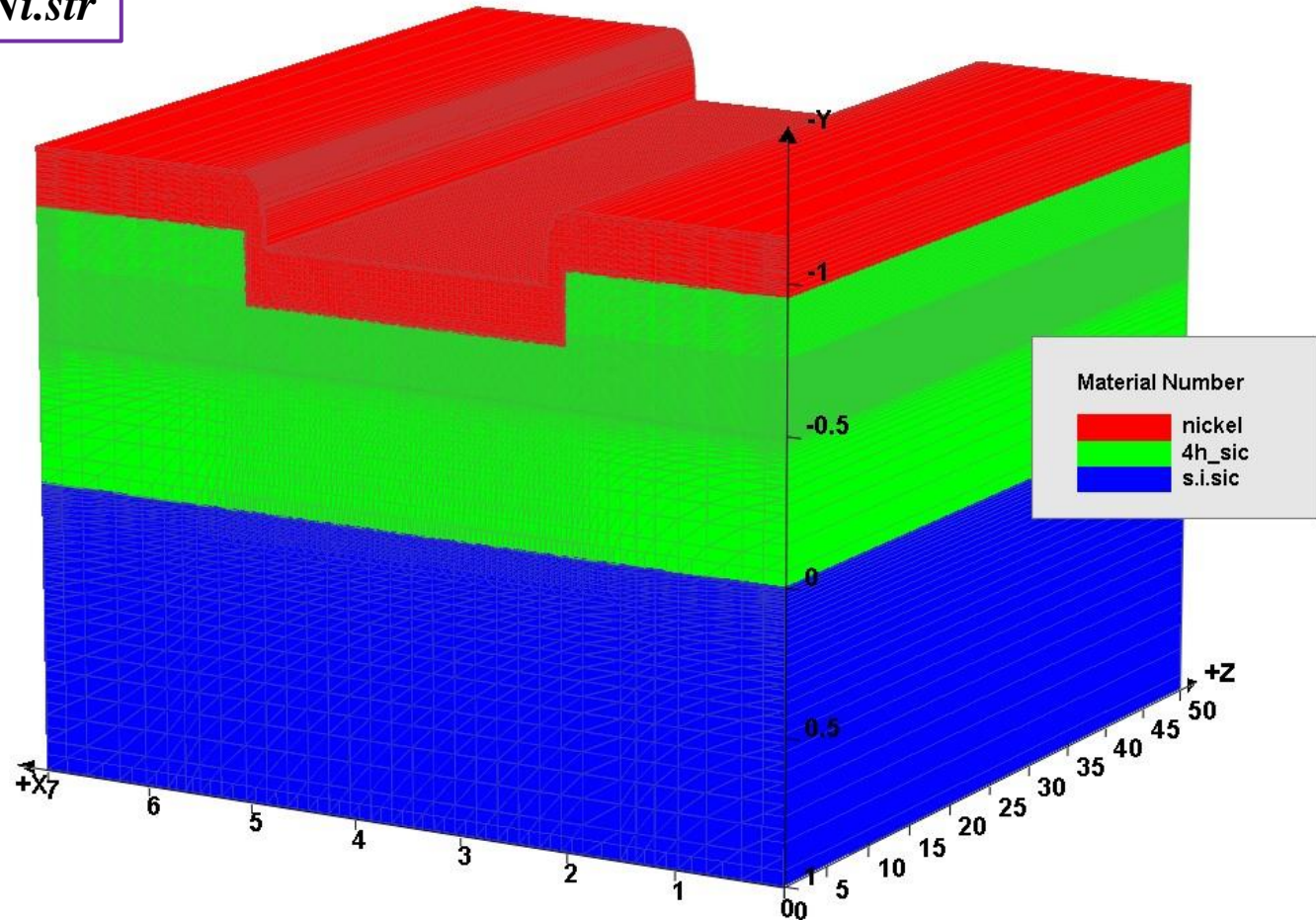
```
include file=mesfet2.msk  
etch dry 4h_sic thick=0.25  
struct outf=03_etch_recesse.str
```



# 3D Process Simulation by CSUPREM

## Step4: deposit nickel

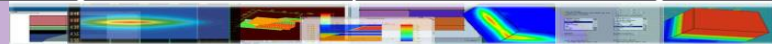
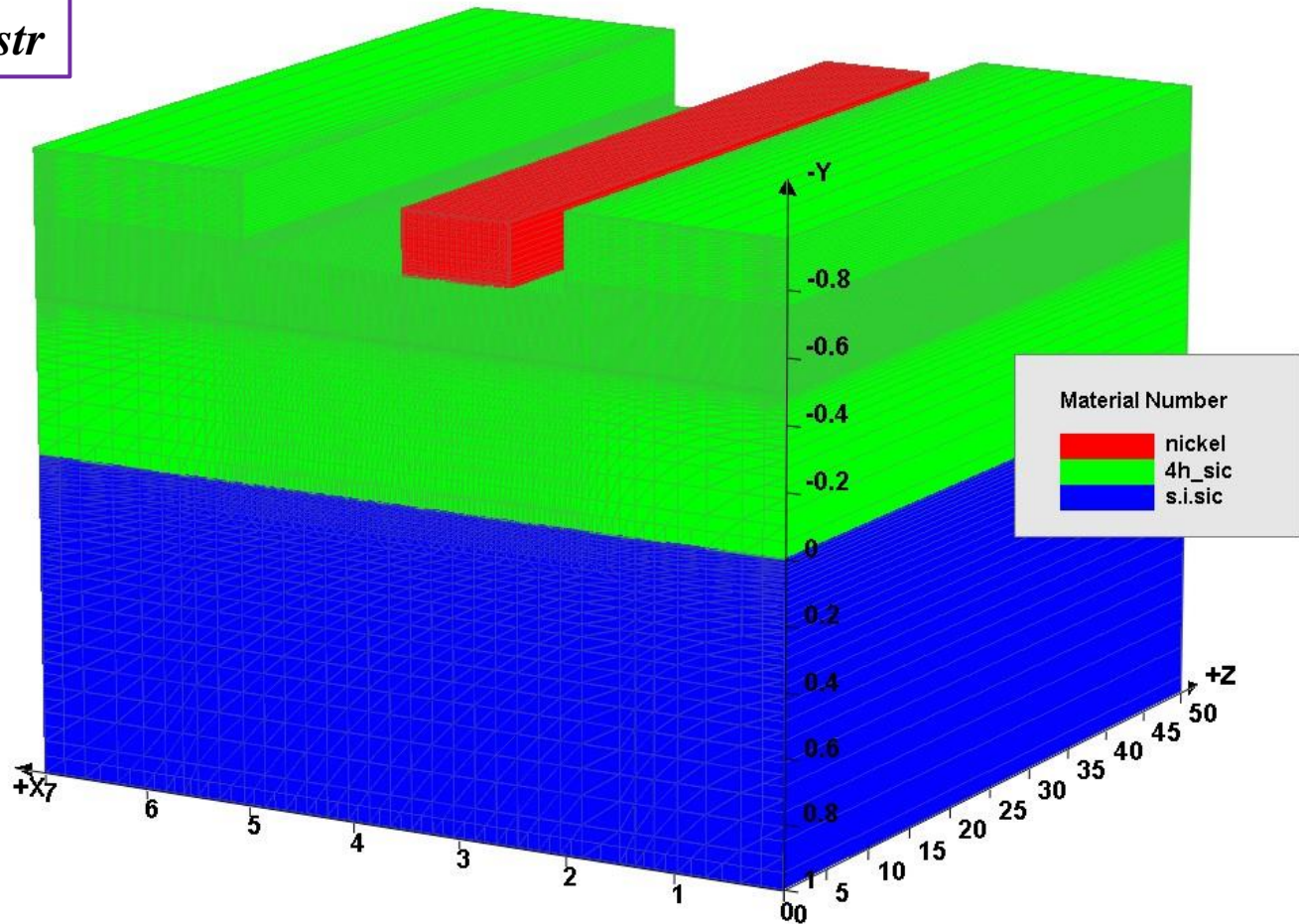
```
deposit nickel thick=0.2  
struct outf=04_deposit_Ni.str
```



# 3D Process Simulation by CSUPREM

## Step 5: lift-off nickel outside the gate area

```
include file=mesfet3.msk  
etch dry nickel thick=1.  
struct outf=05_etch_gate.str
```

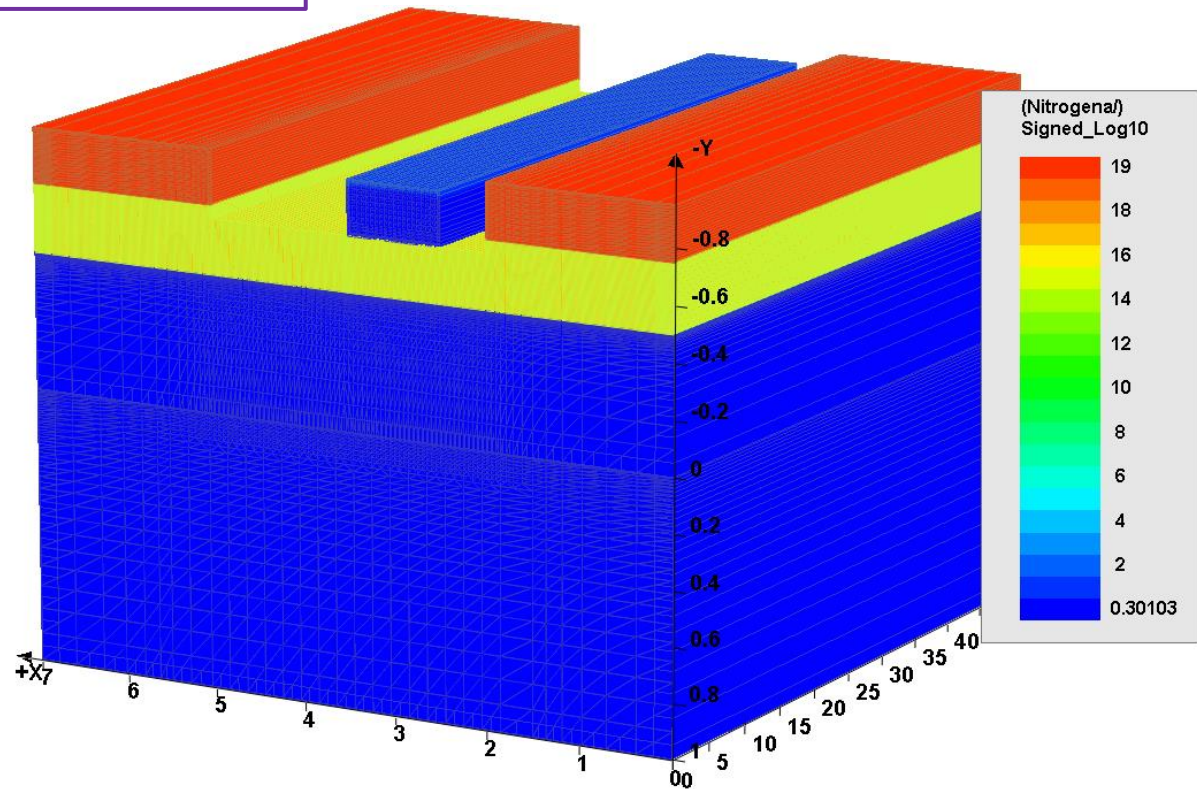




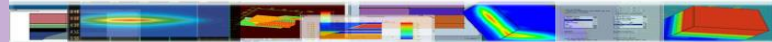
# 3D Process Simulation by CSUPREM

## Step 6: Final 3D structure: **channel-recessed** structure

```
activation.mode al.impurity fraction=1.0  
activation.mode ni.impurity fraction=1.0  
struct outf=06_final.str [1]
```



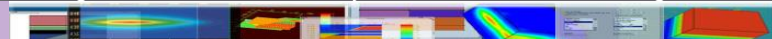
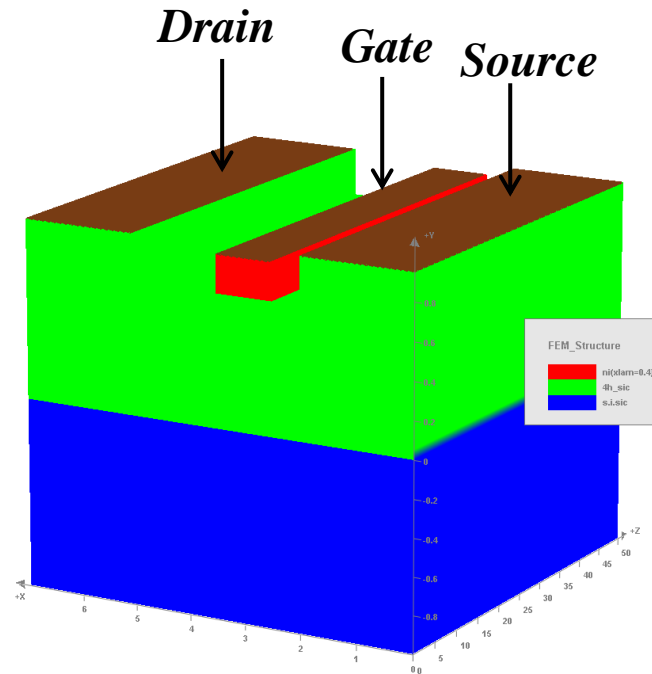
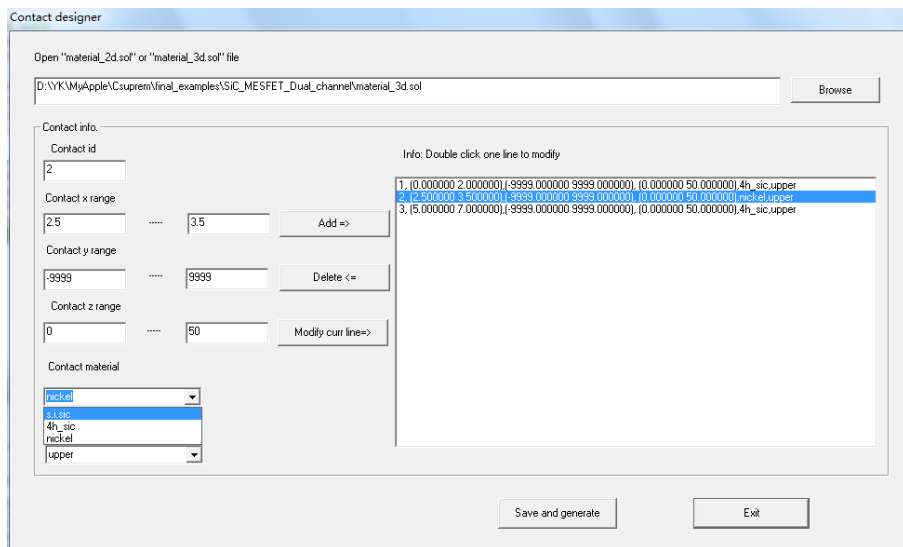
[1] C.L.Zhu et al. Dual-channel 4H-SiC metal semiconductor field effect transistors. *Solid-State Electronics* 51 (2007) 343-346.



# 3D Device Simulation by APSYS

## Set electrode position:

Electrode information is contained in *contact\_3d.sol*



# 3D Device Simulation by APSYS

- Doping dependent mobility model

$$\mu_{oi} = \mu_{1i} + \frac{(\mu_{2i} - \mu_{1i})}{1 + \left(\frac{N_D + N_A + \sum_j N_{tj}}{N_{ri}}\right)\alpha_i} \quad (i = n \text{ or } p)$$

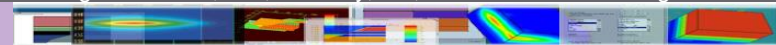
- The Canali model for field dependent mobility

$$\mu_i = \frac{\mu_{oi}}{\left(1 + \left(\frac{\mu_{oi}F}{v_{si}}\right)^{\beta_i}\right)^{\frac{1}{\beta_i}}} \quad (i = n \text{ or } p)$$

- Chynoweth model has been used to calculate impact ionization

$$\alpha = \alpha^\infty e^{-(F_{ci}/F)^{k_i}} \quad (i = n \text{ or } p)$$

- Incomplete ionization of impurities in SiC is important



# 3D Device Simulation by APSYS

- Describe impact ionization parameters in mesfet.sol:

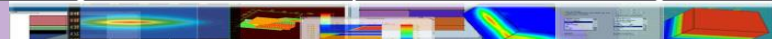
```
impact_chynoweth mater = 2 &&  
hole_setnum = 1 hole_set1 = [3.41e+10,2.50e+09,1.] &&  
elec_setnum = 1 elec_set1 = [9.76e+11,3.30e+09,1.]
```

- Describe interface states between Ni/4H-SiC in mesfet.sol:

```
doping impurity=fix_charge charge_type=negative
```

- Describe traps in 4H-SiC in mesfet.sol:

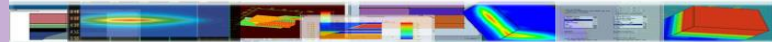
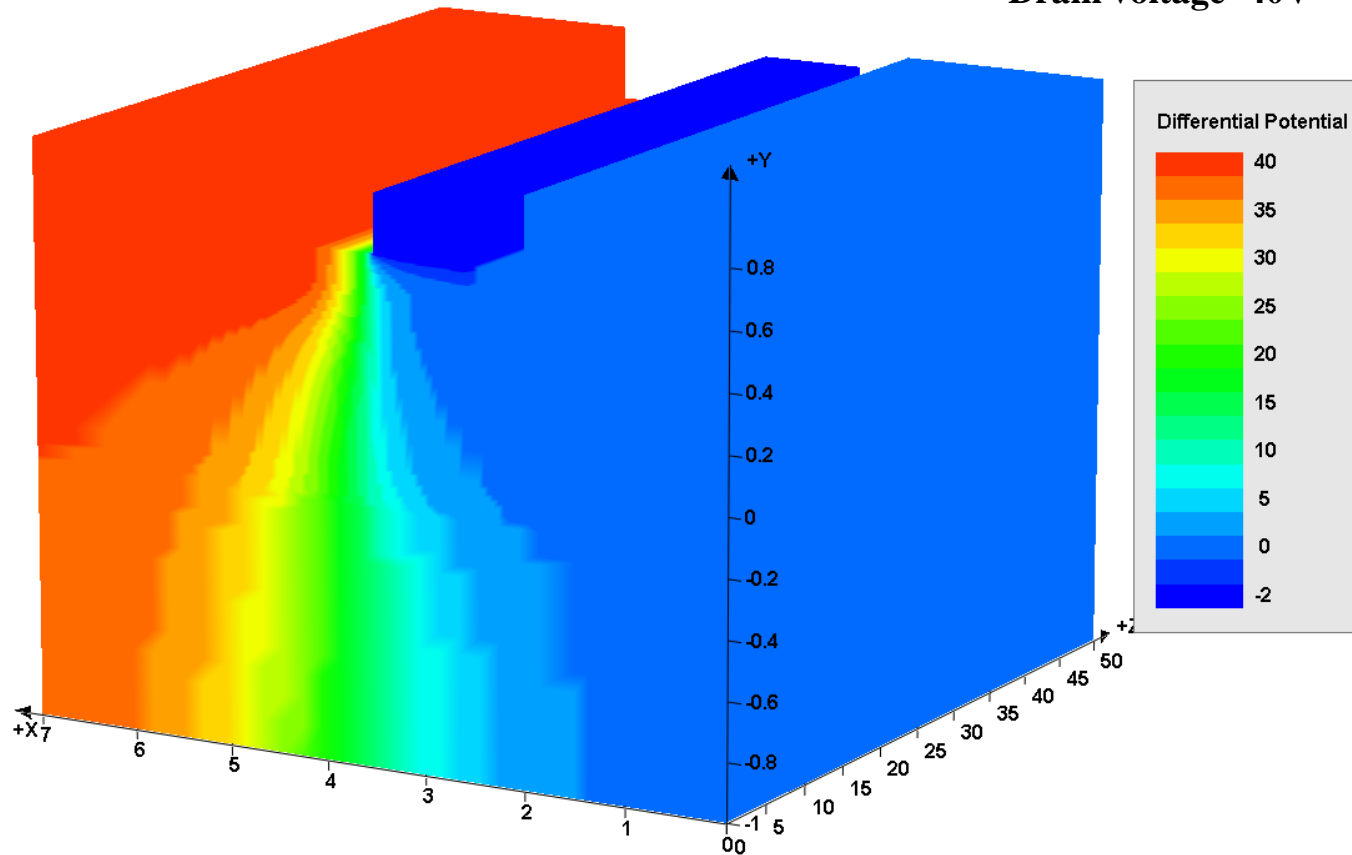
```
doping impurity=trap_1 charge_type=acceptor  
trap_level_1 value=0.400 mater=2  
trap_ncap_1 value=3.e-7 mater=2  
trap_pcap_1 value=3.e-8 mater=2
```



# Simulation Results

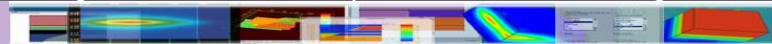
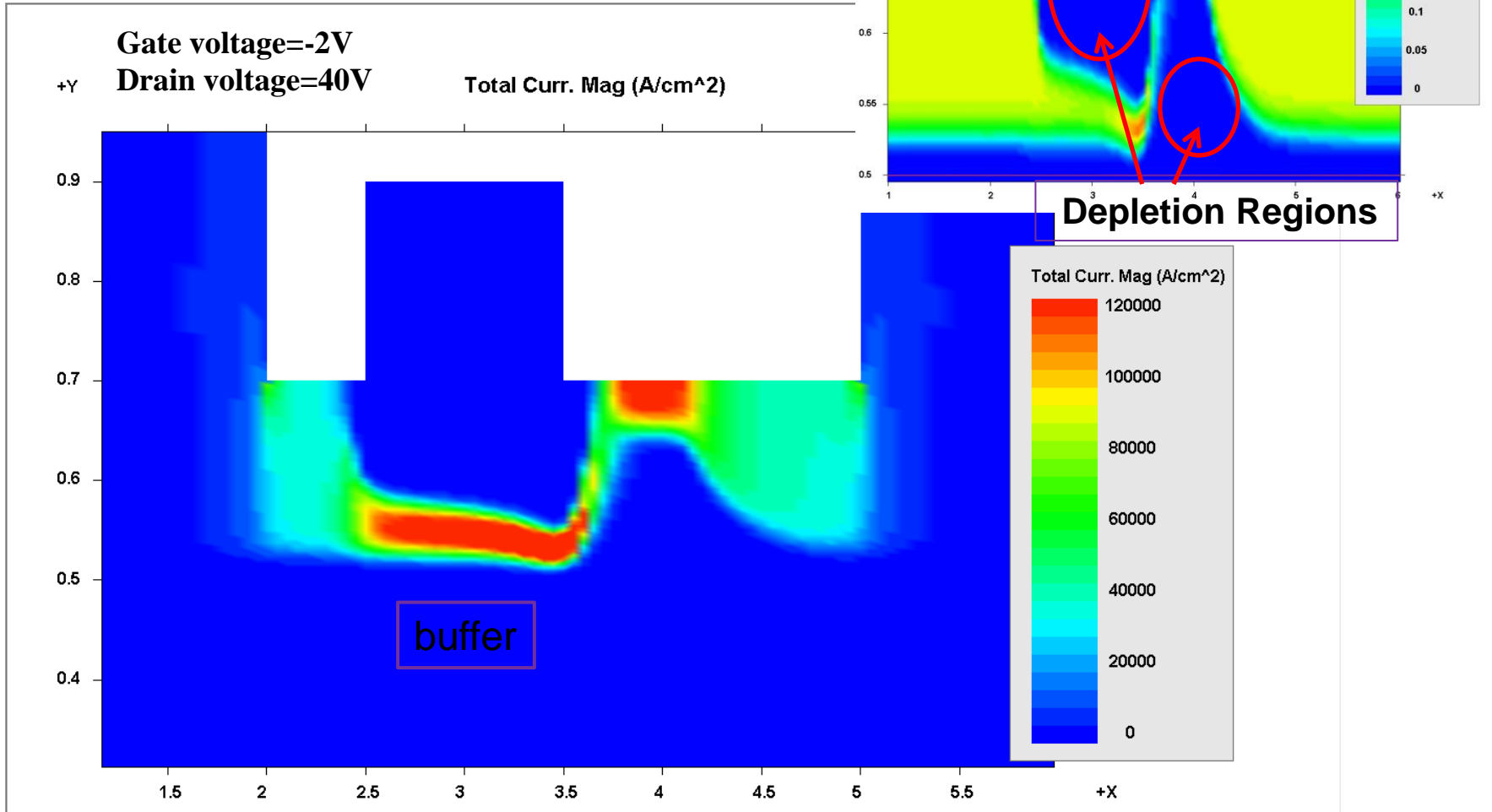
## 3D potential distribution

Gate voltage= -2V  
Drain voltage=40V



# Simulation Results

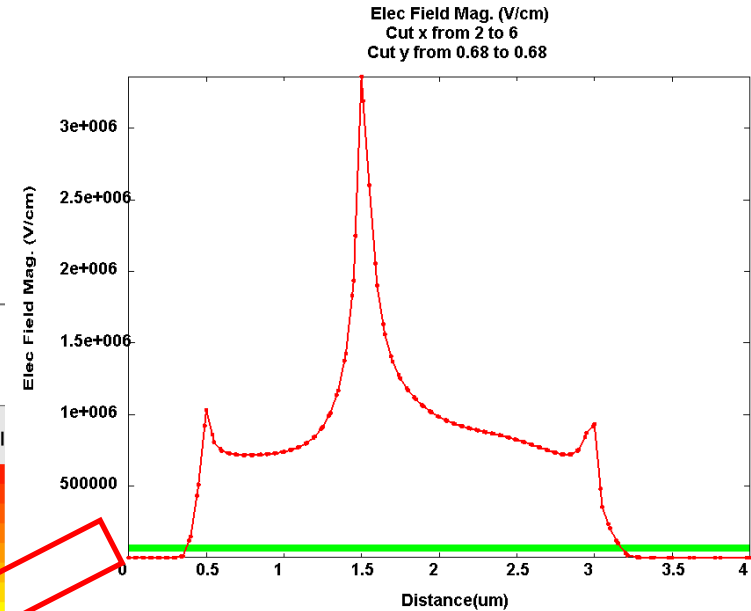
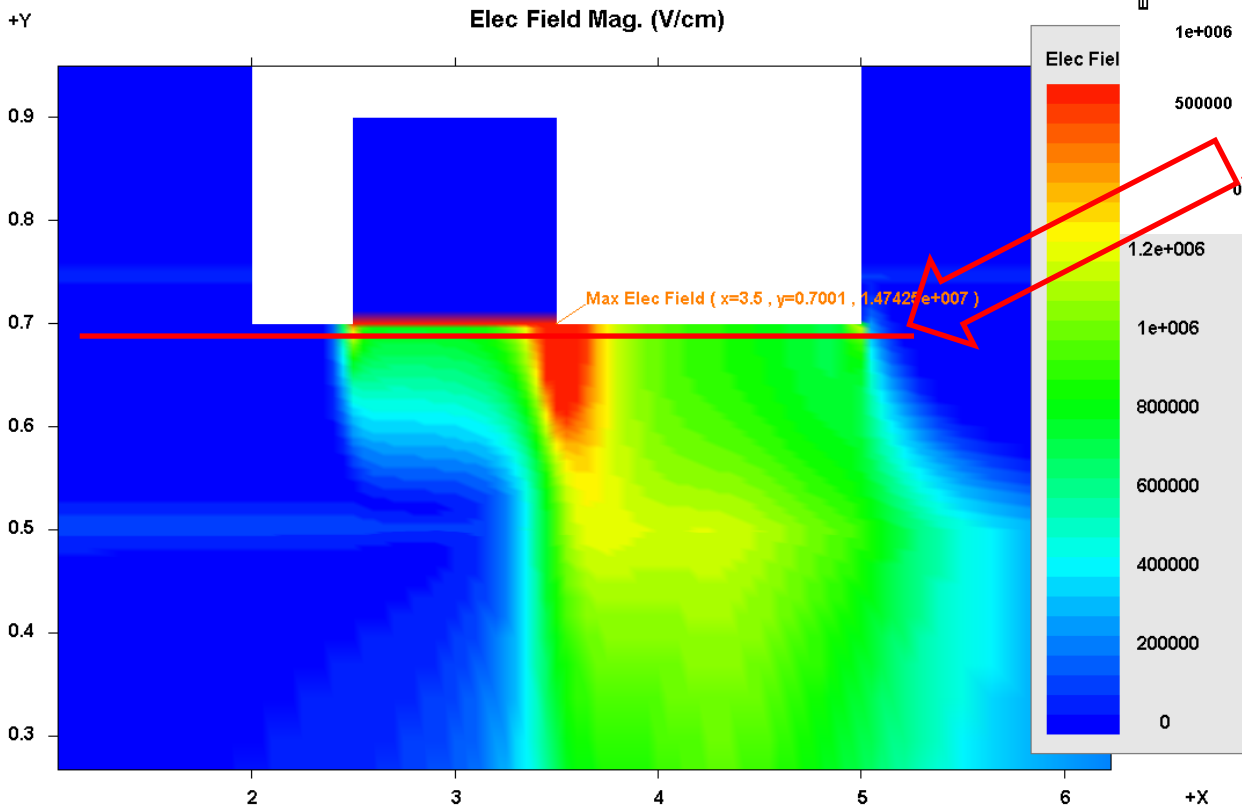
## 2D current distribution



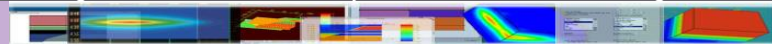
# Simulation Results

## 2D electric field distribution

$V_g = -6V$   $V_d = 160V$



1D cut electric field distribution in the channel region. It shows that the high, sharp peak at the drain side gate edge.

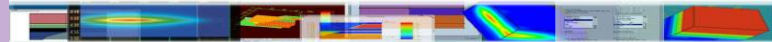
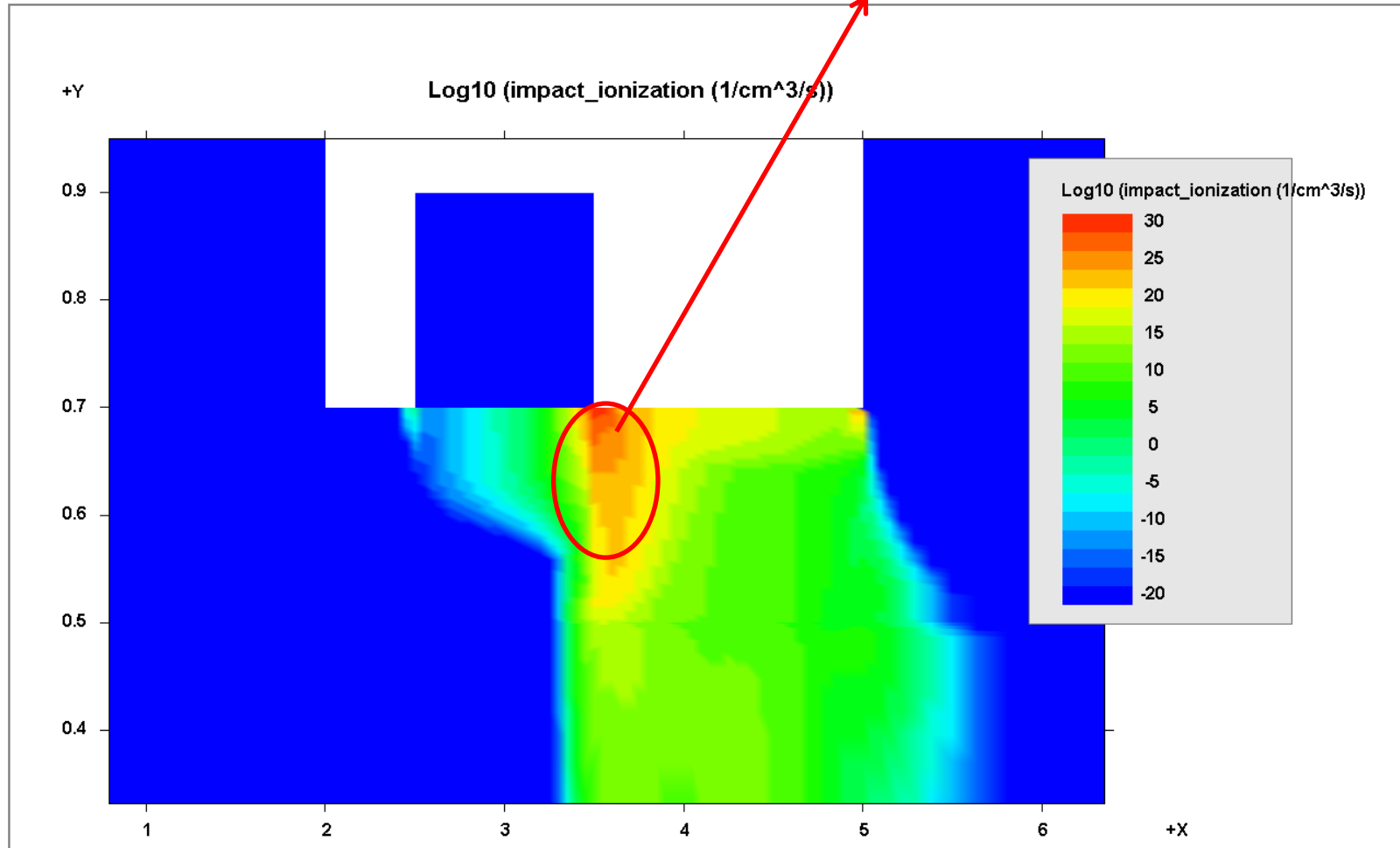


# Simulation Results

## Impact Ionization

$V_g = -6V$   $V_d = 160V$

Gate field emission induced breakdown of the device

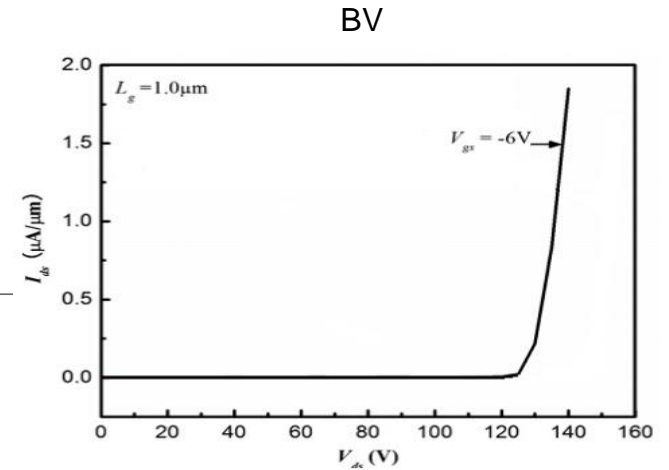
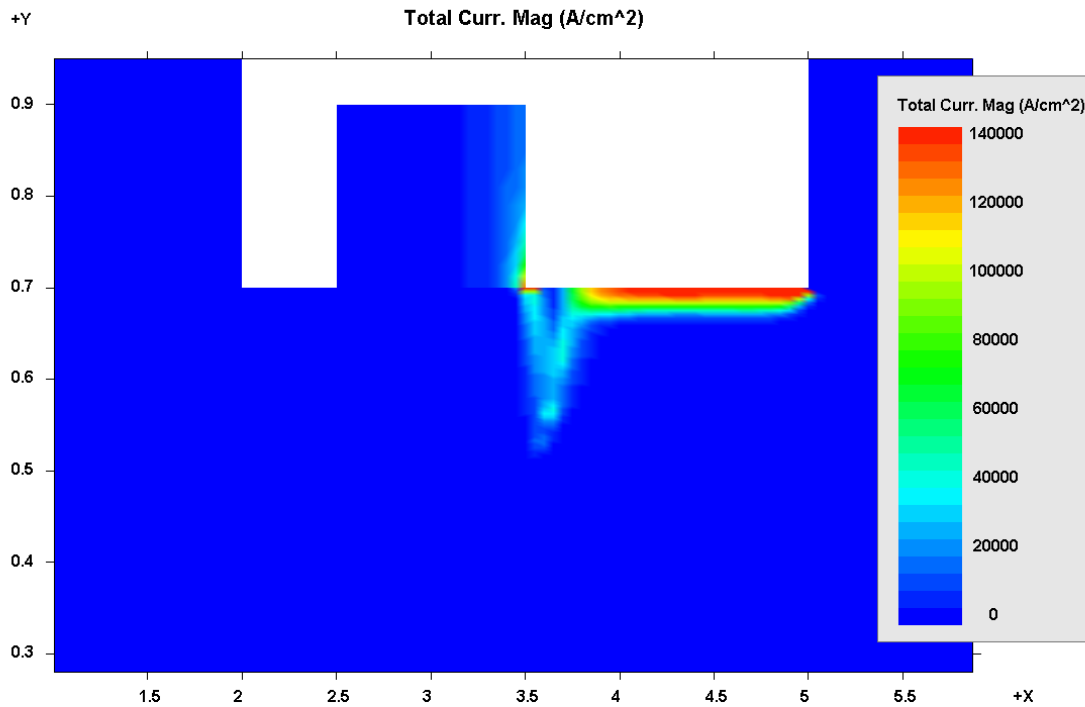




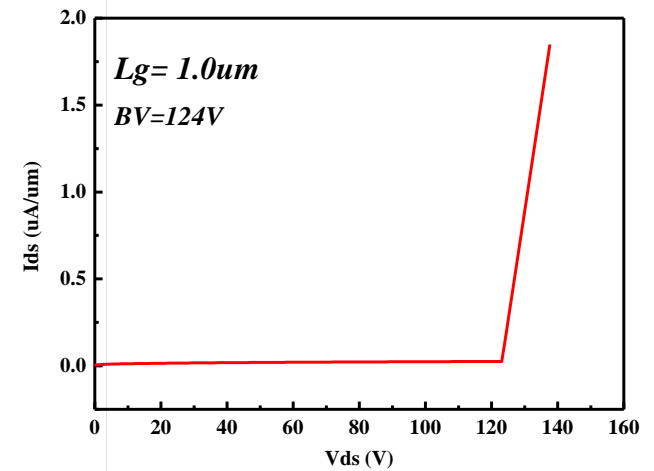
# Simulation Results

## Gate Current after the breakdown

$V_g = -6V$   $V_d = 160V$



## Experimental Result



## Simulation Result

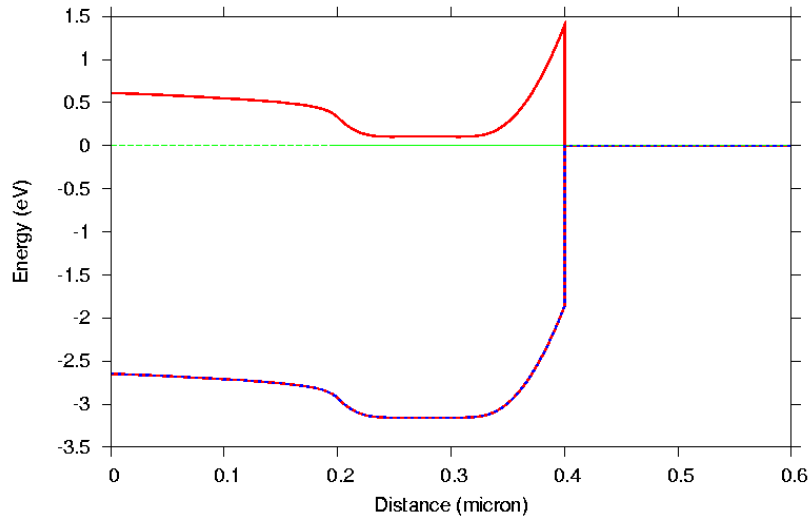


# Simulation Results

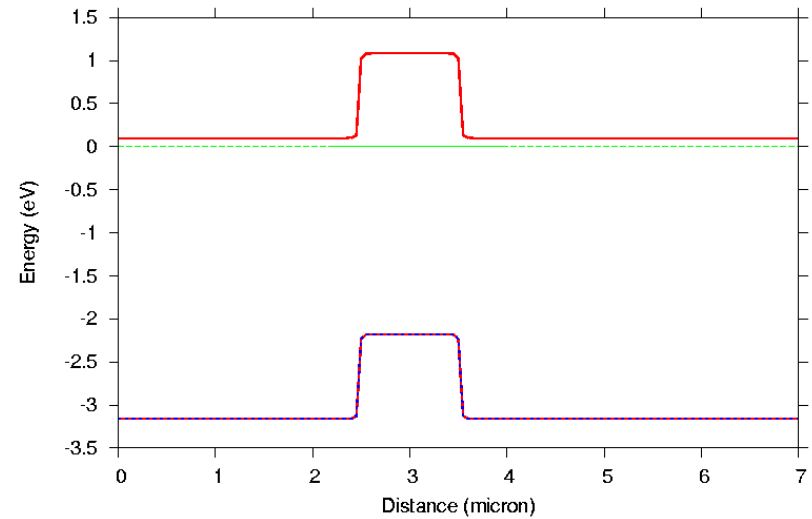
## 1D band diagram

$V_g=0V$   $V_d=0V$

y-direction( $x=0.3$ )

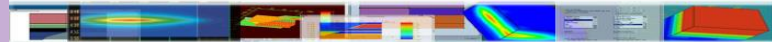
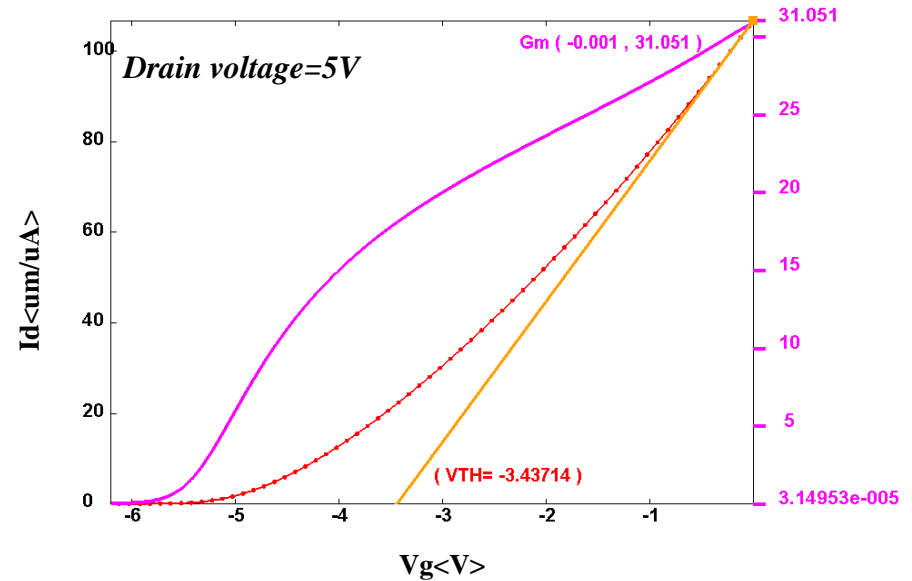
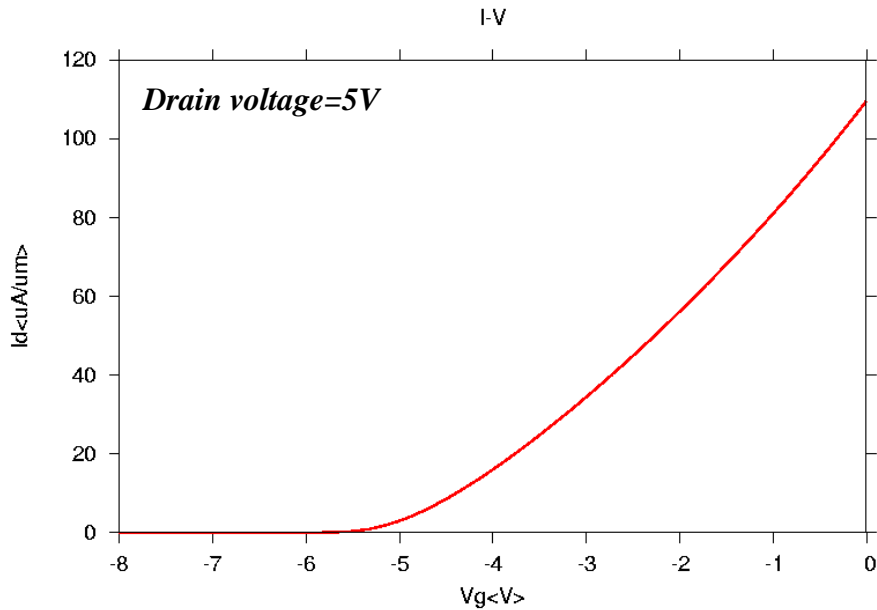


x-direction( $y=0.69$ )



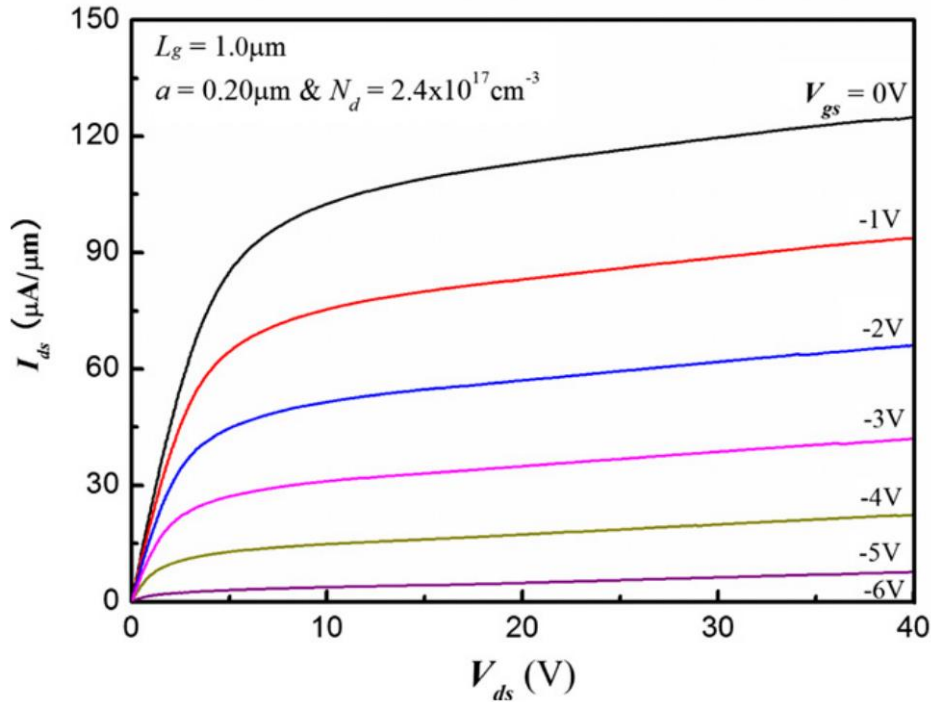
# Simulation Results

## Threshold voltage and $g_m$

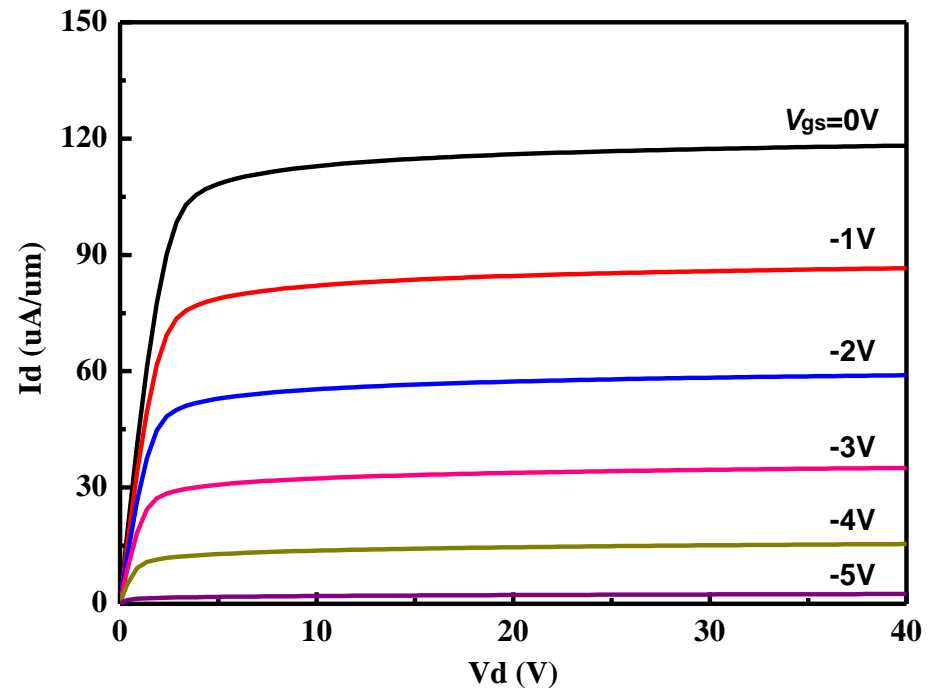


# Simulation Results

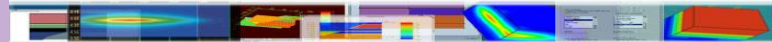
## $I_d$ - $V_d$ family of curves



Experimental Result



Simulation Result



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# CROSSLIGHT

Software Inc.

