GaN Vertical MOSFETs With Monolithically Integrated Freewheeling Merged pn-Schottky Diodes (MPS-MOS) for 1.2-kV Applications

Yuchuan Ma, Heng Wang, Sihao Chen, and Chao Liu

***Abstract*— We report 1.2-kV-class GaN-based vertical trench MOSFETs (T-MOS) with monolithically integrated merged pn-Schottky (MPS) diodes (MPS-MOS) by numerical simulation. The proposed MPS-MOS possesses excellent freewheeling capability, homogenized electric field distribution, as well as enhanced breakdown voltages as compared to conventional GaN vertical T-MOS with intrinsic bipolar body p-i-n diodes. With optimum design parameters by numerical simulation, the MPS-MOS exhibits a reverse turn-on voltage of −0.75 *V* during the third-quadrant operation, a breakdown voltage of 1435 V, and a reduced reverse recovery current (I_{rr}) and charge (Q_{rr}) by 55% and 71%. In addition, a potential approach is provided in this work to suppress the action of the intrinsic body p-i-n diodes, and the principle of the inactivation is explored from the perspective of energy band engineering and carrier distribution modulation. These results reveal great potential of monolithically integrated GaN-based vertical MPS-MOS for high-voltage, high-power density, and high-frequency applications in modern power systems.**

***Index Terms*— Body diode inactivation, breakdown, freewheeling diodes, gallium nitride (GaN), merged pn-Schottky (MPS) diodes, monolithic integration, reverse recovery, Schottky barrier diodes (SBDs), trench MOSFETs, vertical transistors.**

I. Introduction

GALLIUM nitride (GaN) has drawn tremendous attention due to its exceptional properties, such as wide bandgap, large critical electrical field, and high saturation drift velocity. GaN-based power transistors can fulfill the requirements of the next-generation of power electronic systems [1], [2], [3], [4], [5]. Benefiting from the two-dimensional electron gas (2DEG) channel formed at the AlGaN/GaN heterointerface, GaN-based lateral high-electron-mobility-transistors (HEMTs) have been commercialized for medium-power switching applications. Nevertheless, for high-voltage and high-current applications, substantial gate-to-drain spacing of the lateral HEMTs is requisite, which leads to limited switching frequency of the devices due to the existence of additional parasitic elements [6], [7], [8]. In contrast to their lateral counterparts, devices with vertical topologies are capable of achieving higher breakdown voltages by increasing the thickness of the drift layer without enlarging the footprint of the devices. Recently, several types of GaN vertical transistors have been proposed and demonstrated, including junction field-effect transistors (JFETs) [9], [10], [11], [12], current aperture vertical electron transistors (CAVETs) [13], [14], [15], [16], fin power field-effect transistors (FinFETs) [17], [18], [19], and trench MOSFETs (T-MOS) [20], [21], [22], [23], [24], [25], [26], [27]. Among these vertical power transistors, T-MOS are widely researched due to their relatively simple fabrication process and inherent enhancement-mode characteristics with threshold voltages >2 *V*.

For practical application of the emerging vertical transistors in power systems, an extra anti-parallel freewheeling diode is typically demanded to accommodate the reverse current during OFF-state [28], [29], [30]. The intrinsic body p-i-n diodes in GaN T-MOS can provide a freewheeling path to conduct the reverse current. However, the body diodes are supposed to be strictly inactivated due to the large turn-on voltage-induced conduction loss, poor reverse recovery performance, as well as undesirable degradation concerns on account of the continuous bipolar current [31], [32]. By paralleling an external Schottky barrier diode (SBD) with the MOSFETs, the intrinsic body diodes can be bypassed, resulting in superior reverse conduction characteristics in the third quadrant. Nevertheless, the use of the external SBD will consume additional packaging area and introduce a large parasitic inductance, which restricts the high-power and high-frequency applications of the devices [33]. An alternative

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The authors are with the School of Integrated Circuits, Institute of Novel Semiconductors, Shandong Technology Center of Nanodevices and Integration, State Key Laboratory of Crystal Materials, Shandong University, Jinan 250100, China, and also with Shenzhen Research Institute, Shandong University, Shenzhen 518057, China (e-mail: chao.liu@sdu.edu.cn).

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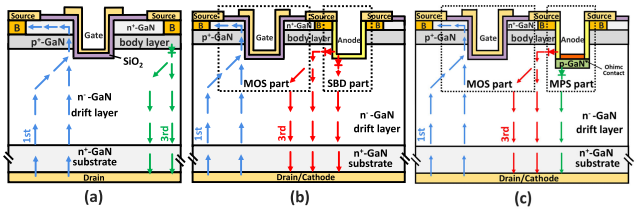

Fig. 1. Cross-sectional schematics of (a) T-MOS, (b) SBD-MOS, and (c) MPS-MOS. The current conduction path in the first and third quadrant is also symboled in the schematics.

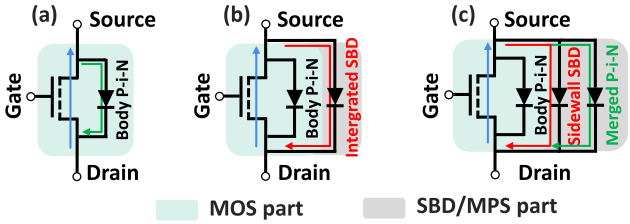

Fig. 2. Equivalent circuits of (a) T-MOS, (b) SBD-MOS, and (c) MPS-MOS.

approach is to integrate the GaN T-MOS and freewheeling SBD on a single chip. Liu et al. [31] reported the world's first monolithically integrated GaN vertical MOSFET-SBDs, which can eliminate the parasitic effects and minimize the volume of power systems. However, the integration of the SBD results in the degraded breakdown capability of the integrated modules due to the barrier lowering issues at the SBD part under high bias conditions.

In this article, we report GaN-based vertical T-MOS with monolithically integrated merged pn-Schottky (MPS) diodes (MPS-MOS) for the purpose of achieving excellent freewheeling and OFF-state breakdown capability simultaneously. With an embedded p-GaN shielding region (p-shielding) at the bottom of the sidewall SBDs, the electric field distribution in the MPS-MOS is uniformly regulated and the Schottky contact surface can be effectively protected from the excessive electric field. As a result, a breakdown voltage of 1435 V can be achieved in the monolithically integrated MPS-MOS, which is a dramatic improvement from 669 V in the MOSFET-SBDs without the p-shielding design (SBD-MOS). In addition, the MPS-MOS exhibits enhanced operation mode with a threshold voltage of 3.7 V, a low turn-on voltage of -0.75 V in the third quadrant, a specific ON-resistance in the third quadrant ($R_{\mathrm{ON,3rd}}$) of 1.41 mΩ·cm^2, and negligible compromise in specific ON-resistance in the first quadrant ($R_{\mathrm{ON,1st}}$). The reverse recovery characteristics (I_{rr} and Q_{rr}) of the integrated MPS-MOS can be effectively reduced by 55% and 71%, as compared to the conventional T-MOS. Furthermore, we propose a potential approach to suppress the action of the body p-i-n diodes and analyze the principle of the inactivation from the perspective of energy band engineering and carrier distribution modulation. These results reveal great potential of monolithically integrated MPS-MOS for future applications in power converters.

II. Device Architectures and Principles

Fig. 1(a)–(c) illustrates the schematic structures of the conventional GaN-based T-MOS, the SBD-MOS, and the proposed MPS-MOS, respectively. From bottom to top, the epitaxial layers of these devices consist of a 13-μm-thick n$^-$-GaN drift region, a 0.7-μm-thick p$^+$-GaN body region, and a 0.2-μm-thick n$^+$-GaN source region on n$^+$-GaN substrates. The T-MOS features an 80-nm-thick SiO_2 as the gate dielectric layer surrounding the gate trenches and nickel (Ni) with a work function of 5.15 eV as the gate electrodes.

The Schottky barrier height (SBH) is determined by the difference between the electron affinity of GaN (4.1 eV) material and the work function of the Schottky electrode material. Pt (5.65 eV), Ni (5.15 eV), and W (4.5 eV) are commonly used as a Schottky anode material, followed by the deposition of Au [34], [35]. Pt with higher work function is used to achieve low leakage current level, but at the expense of high forward voltage drop (V_F). W with lower work function is favorable for realizing smaller V_F and lower conduction loss but results in larger leakage current passing through the Schottky anode. The Schottky electrode material selected in this article is the Ni with a work function of 5.15 eV to develop a Schottky structure with both low leakage current density and low V_F, simultaneously.

The integrated SBD-MOS consists of the MOS part and the SBD part. A trench Schottky anode is formed and integrated with the source pad of the MOS part. The cathode of the SBD part is directly connected with the drain pad through the n$^+$-GaN substrates. Based on the SBD-MOS, a p-GaN structure is introduced underneath the SBD trench to form a p-GaN shielding region in the MPS-MOS, which results in a sidewall Schottky anode in the SBD part. The type of contact between p-shielding and anode is set as ohmic contact.

The current path of the T-MOS and the integrated devices (SBD-MOS and MPS-MOS) is also depicted in Fig. 1. During the first quadrant ON-state operation, the forward current flows through the inversion channel in the MOS part from drain to source [blue arrow line in Fig. 1(a)–(c)]. With inductive load current applied to the devices, the intrinsic body p-i-n diodes in the T-MOS can provide a freewheeling path and conduct the reverse current in a bipolar mode [green arrow line in Fig. 1(a)]. With the integrated trench SBDs in the SBD-MOS, an additional freewheeling path becomes available, which features unipolar-current [red arrow line in Fig. 1(b)] conduction behavior with reduced turn-on voltage in the reverse direction. For the MPS-MOS, by adopting the p-GaN structure at the bottom of the trench, a p-shielding/n-drift junction is merged inside the integrated trench SBD, creating a merged p-i-n Schottky (MPS) diode. The MPS-MOS exhibits the same turn-on voltage as to the SBD-MOS and conducts the reverse freewheeling current from the side wall Schottky anode to the cathode [red arrow line in Fig. 1(c)]. The merged p-n junction not only improves the high surge current robustness of the freewheeling diodes during the third-quadrant operation [green arrow line in Fig. 1(c)] but also protects the Schottky anodes from the excessive electric field during the first-quadrant OFF-state operation [36], [37], [38]. The equivalent circuits of the discrete T-MOS, the integrated SBD-MOS, and MPS-MOS are depicted in Fig. 2(a)–(c), and the current conduction path of the circuits is consistent with that in Fig. 1.

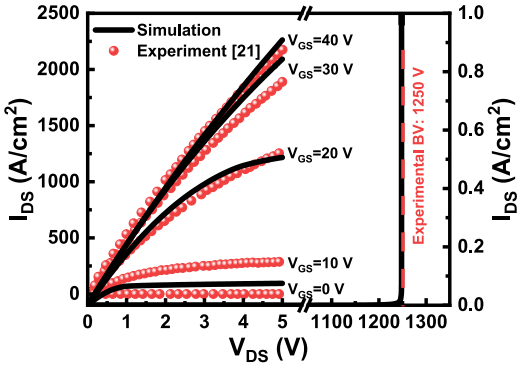

Fig. 3. Simulated and experimental ON-state output I_{DS}–V_{DS} characteristics and OFF-state breakdown I_{DS} – V_{DS} characteristics of the T-MOS [21].

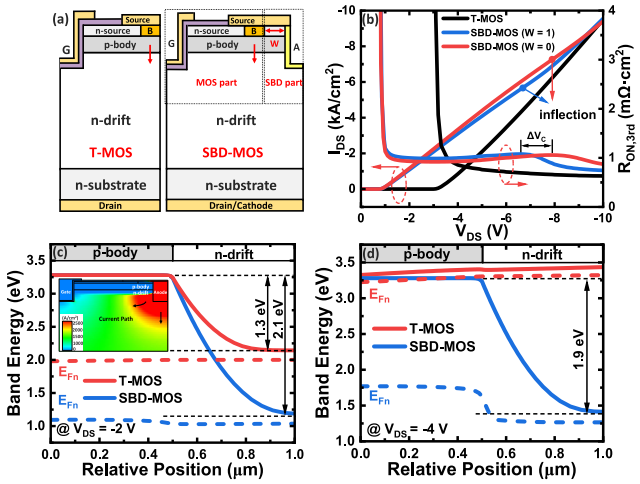

Fig. 4. (a) Enlarged schematics of the discrete T-MOS and integrated SBD-MOS with different W values. (b) Reverse $I_{DS} - V_{DS}$ characteristics of the discrete T-MOS and the integrated SBD-MOS with $W = 1$ μm and 0 μm in the third quadrant. (c) and (d) Conduction band diagrams across the p-body/n-drift junctions and the quasi-Femi levels in the discrete T-MOS and the integrated SBD-MOS ($W = 0$ μm) along the red arrowed lines at $V_{DS} = -2$ and -4 V, respectively. The inset shows the two-dimensional current diagram of the SBD-MOS ($W = 0$ μm) at $V_{DS} = -2$ V.

For the purpose of understanding the working principles of the monolithically integrated SBD/MPS-MOS and exploring the influence of the design parameters on the device performance, TCAD simulations are carried out using the Advanced Physical Models of Semiconductor (APSYS) software. The key physical models include the carrier generation–recombination model, the drift-diffusion model, the continuity and the Poisson equations, the low field mobility model, the electron tunneling model, as well as the impact ionization model. The parameters are calibrated via fitting the ON-state output characteristics and OFF-state breakdown characteristics of the simulated devices with experimental results from [21], as shown in Fig. 3. The good agreements indicate the effectiveness and reasonability of the models and parameters used in this work.

III. Results and Discussion

A. Body Diode Inactivation in the Monolithically Integrated MOSFET-SBDs

When the monolithically integrated MOSFET-SBDs conduct reverse freewheeling current in the third quadrant, the body p-i-n diodes can remain inactivated with the reverse freewheeling current flowing across the Schottky junction. However, there is still a chance for the body diodes to be reactivated subject to large reverse currents from the inductance loads, which may result in shifted threshold voltage and undesirable OFF-state leakage through the MOS channel [39], [40]. Therefore, it is of great significance to avoid the body-diode-related issues in the operation of the monolithically integrated MOSFET-SBDs.

Fig. 4(a) illustrates the enlarged cross-sectional schematics of the discrete T-MOS and the integrated SBD-MOS. The width (W) is labeled as the distance between the edge of the p-body contact and the sidewall of the integrated trench SBDs. Different conduction behaviors of the body p-i-n diodes and integrated SBDs can be observed in the third quadrant with different turn-on voltages for the T-MOS (-3.1 V) and the SBD-MOS (-0.75 V), as shown in Fig. 4(b). Here, we define the critical voltage (V_C) as the drain-to-source bias voltage when it exceeds the built-in potential of the p-body/n-drift junction, which is the turn-on voltage of the body p-i-n diodes for the T-MOS and the inflection point for the SBD-MOS. The inflection point in the SBD-MOS corresponds to the voltage at which the specific ON-resistance starts to drop and the bipolar conduction through the body p-i-n diodes begins to get involved. It can be observed that the SBD-MOS features a much more negative V_C (-6.6 V for $W = 1$ μm and -7.9 V for $W = 0$ μm), as compared to that from the T-MOS (-3.1 V), indicating that the incorporation of the integrated SBDs can effectively suppress the activation of the body p-i-n diodes. We also find that a positive shift in V_C (ΔV_C) of up to 1.3 V can be achieved with reduced W from 1 to 0 μm in the SBD-MOS, which can potentially be utilized to further prohibit the reactivation of the intrinsic body diodes.

For understanding the mechanism behind the suppression of the body p-i-n diodes action in the SBD-MOS, we examined the conduction band diagrams across the p-body/n-drift junction in the T-MOS and SBD-MOS beneath the p-body contacts, along the arrowed lines in Fig. 4(a). The band diagrams were extracted at V_{DS} of -2 and -4 V, which is below and above V_C of the T-MOS (-3.1 V), respectively, as shown in Fig. 4(c) and (d). At $V_{DS} = -2$ V, the drain-to-source bias voltage applied to the T-MOS and the SBD-MOS is not sufficient to overcome the built-in potential of the p-body/n-drift junctions, with the remaining barrier heights of ~1.3 and ~2.1 eV recorded in Fig. 4(c), respectively. The difference in the barrier height can be attributed to the elevated potential induced by the majority carrier flowthrough the sidewall Schottky anodes of the SBD-MOS, as depicted in the inset of Fig. 4(c) [41]. By further increasing V_{DS} to -4 V in Fig. 4(d), the barrier across the p-body/n-drift junction of the discrete T-MOS disappears, while the barrier height persists (~1.9 eV) in the integrated SBD-MOS. We hold this elevated potential to be responsible for the increased value of V_C and the suppression of the body p-i-n diodes action in the integrated SBD-MOS, as compared to the discrete T-MOS.

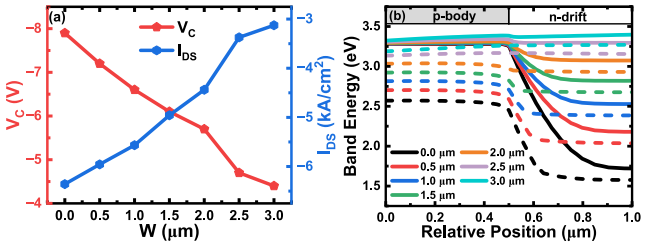

Fig. 5. (a) V_C and I_{DS} (at the inflection point) as a function of the widths (W) between the edge of the body-contact region and the sidewall of the integrated trench SBD in the SBD-MOS. (b) Conduction band diagrams across the p-body/n-drift junction and the quasi-Femi levels with different W values in the integrated SBD-MOS at $V_{DS} = -6$ V.

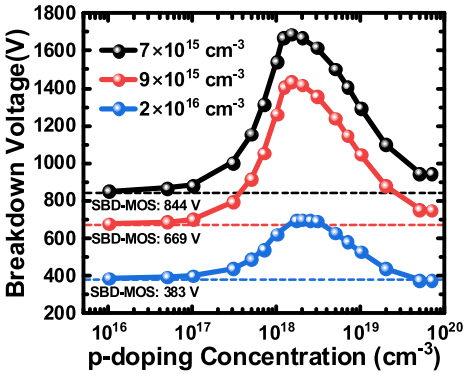

Fig. 6. Breakdown voltage as a function of the doping concentrations in the p-GaN shielding region for the MPS-MOS with different background doping concentrations of 7 × 10^{15} cm^{-3}, 9 × 10^{15} cm^{-3}, and 2 × 10^{16} cm^{-3}, respectively. The p-shielding thickness is set as 0.2 μm.

To further inhibit the activation of the body p-i-n diodes, we varied W in a larger range and extracted the corresponding V_C and I_{DS} at the inflection point of the SBD-MOS, as plotted in Fig. 5(a). With a reduced W, both the values of V_C and I_{DS} increase monotonously. Specifically, by decreasing W to 0 μm with a self-aligned process, V_C of -7.9 V can be obtained in the SBD-MOS, which is far larger than that from the T-MOS (-3.1 V). It is worth noting that the corresponding I_{DS} at inflection point reaches -6358 A/cm^2, which represents the maximum unipolar reverse current density from the inductance loads that can be handled by the integrated SBDs without activating the body p-i-n diodes during the third-quadrant operation. Fig. 5(b) plots the conduction band diagrams across the p-body/n-drift junctions in the SBD-MOS with different W values at $V_{DS} = -6$ V. Elevated barrier heights can be observed across the junction for the SBD-MOS with narrower W, which explains the increased value of V_C as well as the enhanced suppression of the body p-i-n diodes in Fig. 5(a). This can be ascribed to the fact that the density of the current infused from the sidewall Schottky anodes attenuates gradually along the lateral direction. Correspondingly, the energy potential beneath the body p-i-n diodes is affected more severely for the SBD-MOS with narrower W, resulting in increased barrier heights and V_C. Therefore, with optimum design of the monolithically integrated SBD, the body p-i-n diodes can be further inhibited, thus avoiding the undesirable body-diode-related issues.

B. Co-Engineering of the Electric Field Distribution in the Monolithically Integrated MOSFET-SBDs

Based on the results above, the monolithically integrated SBD-MOS exhibits excellent freewheeling ability with stable unipolar conduction mode as well as low turn-on voltage in the third quadrant. However, the integrated SBD-MOS suffers from severe barrier-lowering effect induced by excessive electric field in the SBD part, exhibiting degraded OFF-state breakdown characteristics in the first quadrant compared to the discrete T-MOS. With an embedded p-GaN shielding region in the MPS-MOS, the Schottky contact can be protected from excessive electric field, and the breakdown characteristics of the monolithically integrated MOSFET-SBDs can be boosted. Furthermore, by varying the design parameters (the doping concentration and the thickness) of the p-GaN shielding region, we can homogenize electric field distribution in the MPS-MOS to achieve an optimal OFF-state breakdown performance.

Fig. 6 illustrates the influence of the doping concentrations in the p-GaN shielding region on the breakdown voltage of the MPS-MOS under different background doping concentrations. The breakdown voltage of the SBD-MOS with corresponding background doping concentration is also extracted for comparison, as labeled by the dashed lines. The breakdown voltage is extracted when the OFF-state leakage current density reaches 0.01 A/cm^2 and p-doping concentration in the p-GaN shielding region refers to the ionizable acceptor concentration. The breakdown voltage of the MPS-MOS is inversely proportional to the background doping concentration, which is caused by the reduction of the depletion depth in the n$^-$-GaN drift region during OFF-state. In addition, similar trends in the breakdown voltage can be found for the MPS-MOS with different background doping concentrations, in which the breakdown voltage of the MPS-MOS initially increases and subsequently decreases with increased p-doping concentration. Specifically, a peak breakdown voltage of 1435 V can be achieved for the MPS-MOS at a p-doping concentration of 1.5 × 10^{18} cm^{-3} with a background doping concentration of 9 × 10^{15} cm^{-3}, which is 114.5% larger than that of the SBD-MOS (669 V).

To investigate the mechanisms behind the influence of the p-doping concentration on the OFF-state breakdown characteristics of the MPS-MOS in the first quadrant, the vertical electric field profiles along the dashed line (a–a') are plotted in Fig. 7(a). With a low p-doping concentration of 1 × 10^{17} cm^{-3} in the MPS-MOS, only a minor reduction of the electric field peak can be observed at the trench corner near the Schottky contact, as compared to the SBD-MOS, indicating that the electric field shielding effect from the p-GaN shielding region is insufficient. As the p-doping concentration increases from 1 × 10^{17} cm^{-3} to 1.5 × 10^{18} cm^{-3}, the electric field peak near the Schottky contacts can be effectively reduced, which addresses the tendency for an initially monotonous increase in breakdown voltage at a relatively low p-doping concentration in Fig. 6. In the meantime, the electric field peak moves from the trench corner near the Schottky contact to the vicinity

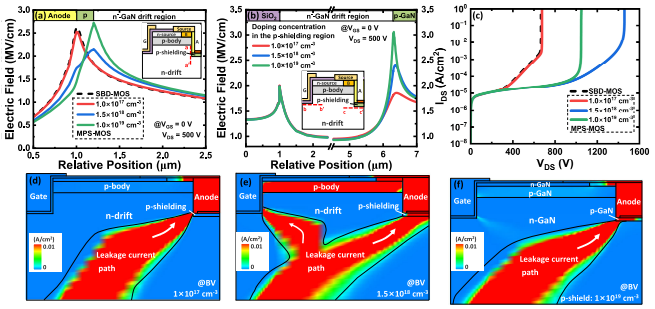

Fig. 7. (a) Electric field profiles along the dashed line (a–a') for the MPS-MOS with different doping concentrations in the p-GaN shielding region at $V_{DS} = 500$ V (the background doping concentration in the n$^-$-GaN drift region: 9×10^{15} cm^{-3}). (b) Electric field profiles along the dashed lines at the bottom of the trench gate (b–b') and p-shielding (c–c') with different p-doping concentrations at $V_{GS} = 0$ V and $V_{DS} = 500$ V (the background doping concentration in the n$^-$-GaN drift region: 9×10^{15} cm^{-3}). (c) Simulated OFF-state breakdown I_{DS}–V_{DS} characteristics of the SBD-MOS and MPS-MOS (p-doping: 1.0×10^{17} cm^{-3}, 1.5×10^{18} cm^{-3}, and 1.0×10^{19} cm^{-3}). (d)–(f) Two-dimensional current diagram of the MPS-MOS at breakdown voltages with the doping concentration of 1×10^{17} cm^{-3}, 1.5×10^{18} cm^{-3}, and 1×10^{19} cm^{-3} in the p-shielding region, respectively.

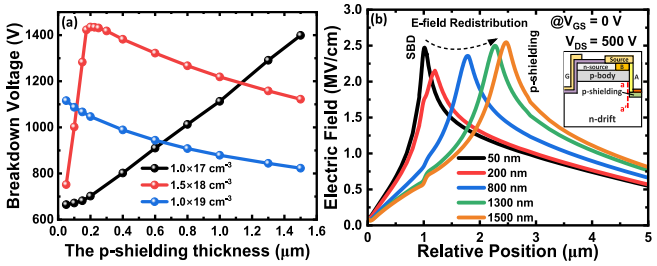

Fig. 8. (a) Breakdown voltage as a function of the p-shielding thickness for the MPS-MOS at a p-doping concentration of 1.0×10^{17} cm^{-3}, 1.5×10^{18} cm^{-3}, and 1.0×10^{19} cm^{-3}, respectively. (b) Electric field profiles along the dashed line (a–a') for the MPS-MOS with different T_p at $V_{GS} = 0$ V and $V_{DS} = 500$ V (the doping concentration in the p-shielding region: 1.5×10^{18} cm^{-3}).

of the p-shielding edge. Further increase in the p-doping concentration to 1×10^{19} cm^{-3} leads to an excessive electric field at the vicinity of the p-shielding edge, which results in premature breakdown of the MPS-MOS and explains the decreasing trend in the breakdown voltage at a relatively high doping concentration in the p-GaN shielding region.

In addition to the vertical electric field distribution in the MPS-MOS, the lateral electric field profiles along the bottom of the gate trench (b–b') and the p-shielding region (c–c') are also illustrated in Fig. 7(b). Two electric field peaks can be observed, corresponding to the corner of the gate trench in the MOS part and the corner of the p-GaN shielding region in the MPS part, respectively. It can be observed that the p-doping level mainly impacts the electric field distribution of the MPS part and has negligible effect on the MOS part. With increased p-doping concentration, the increased value of the electric field can be observed at the corner of p-shielding, which is in agreement with the vertical electric field distribution in Fig. 7(a). Fig. 7(c) plots the OFF-state $I - V$ characteristics in logarithmic scale of the SBD-MOS and MPS-MOS with p-doping concentrations of 1.0×10^{17} cm^{-3}, 1.5×10^{18} cm^{-3}, and 1.0×10^{19} cm^{-3}.

Furthermore, we plot the 2-D current diagrams at breakdown voltage for the MPS-MOS with different p-doping concentrations in Fig. 7(d)–(f). With an insufficient doping concentration of 1.0×10^{17} cm^{-3} in the p-GaN shielding region, breakdown occurs at the corner of the Schottky anodes with leakage current flowing across the Schottky junction, as shown in Fig. 7(d). Further increase in the p-doping concentration to 1.5×10^{18} cm^{-3} leads to an efficient electric field shielding effect; thus, the leakage path across the Schottky contact is nearly eliminated by the p-GaN shielding region. In the meantime, the laterally uniform distribution of the electric field results in simultaneous breakdown and OFF-state leakage current at the trench gate corners of the MOS part and the p-shielding edges of the SBD part, as shown in Fig. 7(e).

The electric field crowding effect occurs at the vicinity of the p-shielding edge with a high p-doping concentration of 1×10^{19} cm^{-3}, resulting in premature breakdown of the MPS-MOS. Thus, the majority of the leakage current at the breakdown voltage flows through the corner of the p-GaN shielding region to the source pad, and a small proportion of the leakage current is discovered flowing through the trench gate corner to the source pad in Fig. 7(f). As a result, by optimizing the doping concentration in the p-GaN shielding region, the Schottky anode can be effectively protected from the excessive electric field and the electric field distribution in the MOS part and the SBD part can be co-optimized, leading to a dramatic improvement in the OFF-state breakdown characteristics.

Except for the doping concentration in the p-GaN shielding region, the p-shielding thickness (T_p) also plays a vital role in the breakdown characteristics of the monolithically integrated MPS-MOS during OFF-state. As illustrated in Fig. 8(a), subject to different p-doping concentrations, the influence of T_p on the breakdown characteristics varies. For a relatively high p-doping concentration of 1×10^{19} cm^{-3}, the breakdown voltage of the MPS-MOS decreases monotonously with T_p. With a doping concentration of 1.5×10^{18} cm^{-3} in the p-shielding region, the breakdown voltage of the MPS-MOS first increases and then decreases with the increased T_p. A maximum breakdown voltage of 1435 V is obtained at T_p of 0.2 μm. Further decreasing the doping concentration in the p-shielding to 1×10^{17} cm^{-3}, the breakdown voltage of the MPS-MOS is positively correlated with T_p, indicating that a relatively larger thickness of the p-shielding is preferred for the MPS-MOS with a lower p-doping concentration to enhance the breakdown voltage of the device. In order to analyze and explain the trend mentioned above, we intercepted the vertical electric field profiles in the MPS-MOS along the dashed line (a–a'), as shown in Fig. 8(b). The peak value of the electric field near the Schottky anode first decreases, and then, a gradually increased electric field near the p-shielding edge can be found with increased T_p, which agrees with the breakdown tendency in Fig. 8(a).

In addition, the breakdown voltage of the MPS-MOS as a function of the trench width (X) and depth (Y) in the MPS part is illustrated in Fig. 9(a). With increased X, a sharp increase of the breakdown voltage from 1230 V (Device A1) to 1435 V

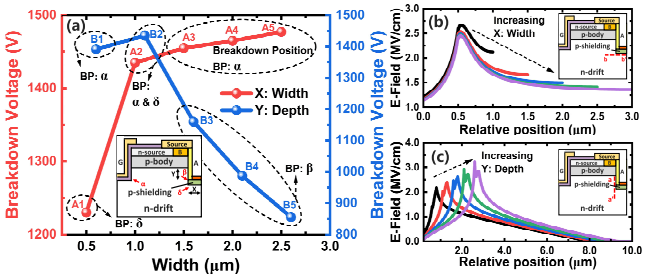

Fig. 9. (a) Breakdown voltage as a function of the width (X) and depth (Y) of the trench in the MPS part for the MPS-MOS. The inset shows the potential BP in the MPS-MOS. (b) Electric field profiles along the dashed line (b–b') for the MPS-MOS with different X values at $V_{GS} = 0$ V and $V_{DS} = 500$ V. (c) Electric field profiles along the dashed line (a–a') for the MPS-MOS with different Y values at $V_{GS} = 0$ V and $V_{DS} = 500$ V.

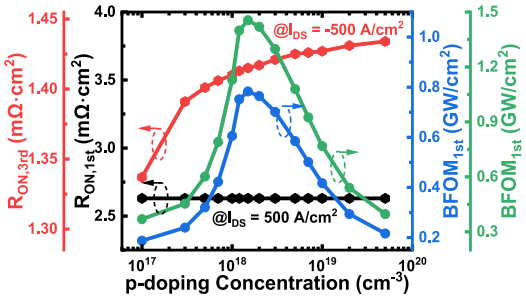

Fig. 10. Extracted R_{ON} and BFOM of the MPS-MOS in the first and third quadrant as a function of doping concentration in the p-shielding region (the p-shielding thickness: 0.2 μm).

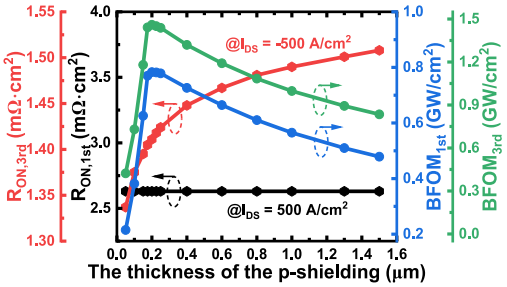

Fig. 11. Extracted R_{ON} and BFOM of the MPS-MOS in the first and third quadrant as a function of the p-shielding thickness (the doping concentration in the p-GaN shielding region: 1.5×10^{18} cm^{-3}).

(Device A2) can be observed, followed by a gradual growth from Devices A2 to A5. Considering the complexity of the electric distribution in the monolithically integrated devices, we also labeled the corresponding breakdown position (BP) for each X and Y, based on the leakage path at breakdown voltages. The BP gradually shifts from the vicinity of the p-shielding edge (point δ) to the gate trench corner (point α) with increased X. On the other hand, the breakdown voltage of the MPS-MOS initially increases and subsequently decreases with increased Y. The corresponding BP eventually shifts from point α to the Schottky anode (point β). To investigate the mechanisms behind the influences of X and Y on the breakdown voltage and BP of the MPS-MOS, we plot the lateral electric field profiles with different X values along the dashed line (b–b') and vertical electric field profiles with different Y values along the dashed line (a–a'), respectively. Fig. 9(b) illustrates an obvious reduction in the peak electric field with X increased from 0.5 μm (Device A1) to 1 μm (Device A2), while the peak electric field remains nearly the same with further increased X up to 2.5 μm (Devices A2–A5). The redistribution process of the electric field agrees with the variation trend of the breakdown voltages with different X values. With increased Y in Fig. 9(c), the peak value of the electric field near the Schottky anode increases monotonically, which explains the degraded breakdown voltage from B2 to B5 in Fig. 9(a). The slightly degraded breakdown voltage in Device B1 as compared to Device B1 can be attributed to the weakened electrostatic interaction between the gate trench and SBD trench [42].

After addressing the impact of the design parameters on the breakdown characteristics of the monolithically integrated MOSFET-SBDs, we then investigate the influence of the doping concentration and thickness of the p-GaN shielding region on the forward and reverse conduction characteristics of the MPS-MOS in the first and third quadrants. $R_{ON,1st}$ of the MOS part in the first quadrant and $R_{ON,3rd}$ of the SBD part in the third quadrant are extracted in Fig. 10. The value of $R_{ON,1st}$ remains at 2.63 mΩ·cm^2 with increased doping concentration in the p-GaN shielding region, while the value of $R_{ON,3rd}$ increases monotonously with the p-doping concentration. Moreover, we calculate and compare the Baliga's figure of merit value (BFOM $=$ BV^2/R_{ON}) for the MPS-MOS in the first quadrant (BFOM$_{1st}$) and third quadrant (BFOM$_{3rd}$). With the increase of the p-doping concentration, the values of BFOM$_{1st}$ and BFOM$_{3rd}$ first increase and then decrease, with the maximum values recorded at a doping concentration of 1.5×10^{18} cm^{-3} in the p-GaN shielding region, which corresponds to the maximum breakdown voltage of the MPS-MOS.

Fig. 11 plots the relationship between R_{ON}, BFOM, and T_p. A similar trend of the forward and reverse conduction characteristics can be observed with the increased T_p, in which $R_{ON,1st}$ remains nearly constant while $R_{ON,3rd}$ increases monotonously from 1.34 to 1.51 mΩ·cm^2 with T_p from 0.05 to 1.3 μm. The maximum BFOM$_{1st}$ and BFOM$_{3rd}$ of 0.78 and 1.46 GW/cm^2 can be obtained in the MPS-MOS with a doping concentration of 1.5×10^{18} cm^{-3} in the p-GaN shielding region and a T_p of 0.2 μm, which features 358.82% and 215.21% enhancement as compared to the values from the SBD-MOS.

C. I–V and Reverse Recovery Characteristics of the Discrete MOSFET and Monolithically Integrated MOSFET-SBDs

Fig. 12 presents the optimum static performance of the monolithically integrated MOSFET-SBDs (SBD-MOS and MPS-MOS), including the forward conduction and OFF-state breakdown characteristics in the first quadrant as well as the reverse conduction in the third quadrant. The forward and reverse I_{DS}–V_{DS} characteristics of the discrete T-MOS are also plotted for comparison. During the third-quadrant reverse conduction operation, the SBDs integrated in the SBD-MOS and MPS-MOS conduct the reverse current in a unipolar mode

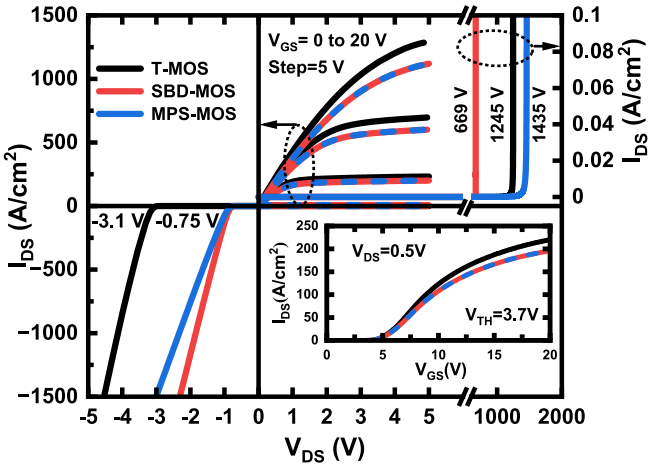

Fig. 12. Forward conduction and OFF-state breakdown characteristics in the first quadrant and reverse conduction in the third quadrant of the T-MOS, SBD-MOS, and the optimum MPS-MOS. The inset shows the transfer characteristics ($I_{DS} - V_{GS}$) of the T-MOS, SBD-MOS, and the MPS-MOS at $V_{DS} = 0.5$ V.

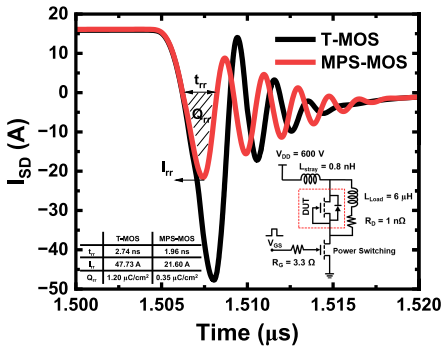

Fig. 13. Simulated reverse recovery characteristics of the T-MOS and the MPS-MOS. The inset shows the double pulse testing circuit for reverse recovery characteristics at $V_{DD} = 600$ V.

with a turn-on voltage of -0.75 V, which is much smaller than that of the body p-i-n diodes in the T-MOS (-3.1 V). A minor increase of the $R_{ON,3rd}$ can be observed in the MPS-MOS as compared with the SBD-MOS due to the reduced Schottky junction area with embedded p-GaN shielding region.

When it comes to the first-quadrant forward conduction operation, the forward current of these devices flows through inversion channel in the MOS part from drain to source when V_{GS} exceeds the threshold voltage ($V_{TH} = 3.7$ V). All devices exhibit good saturation behaviors. The ON-state current density at $V_{GS} = 20$ V and $V_{DS} = 5$ V is $\sim$1.29 kA/cm^2 for the T-MOS and $\sim$1.11 kA/cm^2 for the SBD-MOS and the MPS-MOS, respectively. Correspondingly, the specific ON-resistance of the MOS part in the first-quadrant ($R_{ON,1st}$) estimated from the linear region is 2.38 m$\Omega\cdot$cm^2 for T-MOS and 2.63 m$\Omega\cdot$cm^2 for SBD-MOS and MPS-MOS, respectively. The slightly increased specific ON-resistance is attributed to lower channel density induced by the extension of the cell pitch in the monolithically integrated MOSFET-SBDs, which also reduces the saturation current density. In addition, as shown in the inset of Fig. 12, the integrated devices (MOS-SBD and MPS-MOS) show normally-OFF (E-mode) operation with the same threshold voltage (V_{TH}) of $\sim$3.7 V (obtained at $I_{DS} = 0.1$ A/cm^2) as the discrete device (T-MOS), indicating that the integrated SBDs have no influences on the MOS inversion channel.

During the first-quadrant OFF-state operation mode, the inversion channel in the MOS part is blocked at $V_{GS} = 0$ V. With an embedded p-GaN shielding region underneath the trench in the SBD part, the sidewall Schottky anode in the MPS-MOS can be shielded from excessive electric field, leading to an enormous enhancement in the breakdown voltage to 1435 V, as compared to that of the SBD-MOS (669 V). Please note that the MPS-MOS exhibits an even larger breakdown voltage than that of the T-MOS (1245 V). This is attributed to the fact that the electric field in the monolithically integrated MOSFET-SBD is redistributed laterally. Eventually, we obtain monolithically integrated MOSFET-SBDs with boosted breakdown voltage of 1435 V, excellent freewheeling capability in the third quadrant, and negligible compromise in the first quadrant characteristics.

Fig. 13 shows the reverse recovery current waveforms of the T-MOS and the MPS-MOS. The inset shows the double-pulse testing circuit, in which the device under test (DUT) is set at the upper arm. The integrated MPS-MOS features a peak reverse recovery current (I_{rr}) of 21.60 A, a reverse recovery charge (Q_{rr}) of 0.35 μC/cm^2, and a reverse recovery time (t_{rr}) of 1.96 ns, which is 55%, 71%, and 28% smaller than that of the conventional T-MOS (47.73 A, 1.20 μC/cm^2, and 2.74 ns). The superior reverse recovery characteristics can be attributed to the fact that the bipolar freewheeling conduction through the intrinsic p-i-n body diodes is successfully inhibited with integrated MPS diodes [43].

IV. Conclusion

In summary, we propose a 1.2-kV-class vertical GaN MPS-MOS design strategy, simultaneously achieving excellent freewheeling capability, OFF-state breakdown characteristics, and reverse recovery performance in the monolithically integrated devices by numerical simulation. The undesired body-diode-related issues are also eliminated by integrating an MPS diode with the conventional T-MOS. We believe that the results are very promising for the future application of GaN vertical MOSFETs in the next generation of high-efficiency power electronic systems.

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References

[1] T. P. Chow and R. Tyagi, "Wide bandgap compound semiconductors for superior high-voltage unipolar power devices," *IEEE Trans. Electron Devices*, vol. 41, no. 8, pp. 1481–1483, Aug. 1994, doi: 10.1109/16.297751.

[2] J. Hu, Y. Zhang, M. Sun, D. Piedra, N. Chowdhury, and T. Palacios, "Materials and processing issues in vertical GaN power electronics," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 75–84, May 2018, doi: 10.1016/j.mssp.2017.09.033.

[3] H. Fu, K. Fu, S. Chowdhury, T. Palacios, and Y. Zhao, "Vertical GaN power devices: Device principles and fabrication technologies—Part I," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3200–3211, Jul. 2021, doi: 10.1109/TED.2021.3083239.

[4] H. Fu, K. Fu, S. Chowdhury, T. Palacios, and Y. Zhao, "Vertical GaN power devices: Device principles and fabrication technologies—Part II," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3212–3222, Jul. 2021, doi: 10.1109/TED.2021.3083209.

[5] H. Ishida et al., "GaN-based semiconductor devices for future power switching systems," in *IEDM Tech. Dig.*, Dec. 2016, pp. 20.4.1–20.4.4, doi: 10.1109/IEDM.2016.7838460.

[6] Y. Zhang et al., "Electrothermal simulation and thermal performance study of GaN vertical and lateral power transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2224–2230, Jul. 2013, doi: 10.1109/TED.2013.2261072.

[7] K. J. Chen et al., "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.

[8] L. Nela et al., "Multi-channel nanowire devices for efficient power conversion," *Nature Electron.*, vol. 4, no. 4, pp. 284–290, Mar. 2021, doi: 10.1038/s41928-021-00550-8.

[9] D. Ji and S. Chowdhury, "Design of 1.2 kV power switches with low R ON using GaN-based vertical JFET," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2571–2578, Aug. 2015, doi: 10.1109/TED.2015.

[10] C. Yang et al., "GaN vertical-channel junction field-effect transistors with regrown p-GaN by MOCVD," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 3972–3977, Oct. 2020, doi: 10.1109/TED.2020.3010183.

[11] S. Kotzea, A. Debald, M. Heuken, H. Kalisch, and A. Vescan, "Demonstration of a GaN-based vertical-channel JFET fabricated by selective-area regrowth," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5329–5336, Dec. 2018, doi: 10.1109/TED.2018.2875534.

[12] H. Nie et al., "1.5-kV and 2.2-mΩ-cm^2 vertical GaN transistors on bulk-GaN substrates," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 939–941, Sep. 2014, doi: 10.1109/LED.2014.2339197.

[13] R. Yeluri et al., "Design, fabrication, and performance analysis of GaN vertical electron transistors with a buried p/n junction," *Appl. Phys. Lett.*, vol. 106, no. 18, May 2015, Art. no. 183502, doi: 10.1063/1.4919866.

[14] D. Shibata et al., "1.7 kV/1.0 mΩcm^2 normally-off vertical GaN transistor on GaN substrate with regrown p-GaN/AlGaN/GaN semipolar gate structure," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2016, pp. 10.1.1–10.1.4, doi: 10.1109/IEDM.2016.7838385.

[15] D. Ji, A. Agarwal, H. Li, W. Li, S. Keller, and S. Chowdhury, "880 V/2.7 mΩ·cm^2 MIS gate trench CAVET on bulk GaN substrates," *IEEE Electron Devices Lett.*, vol. 39, no. 6, pp. 863–865, Jun. 2018, doi: 10.1109/LED.2018.2828844.

[16] M. Kanechika et al., "A vertical insulated gate AlGaN/GaN heterojunction field-effect transistor," *Japanese J. Appl. Phys.*, vol. 46, no. 6L, p. L503, May 2007, doi: 10.1143/jjap.46.l503.

[17] M. Sun, Y. Zhang, X. Gao, and T. Palacios, "High-performance GaN vertical fin power transistors on bulk GaN substrates," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 509–512, Apr. 2017, doi: 10.1109/LED.2017.2670925.

[18] Y. Zhang et al., "1200 V GaN vertical fin power field-effect transistors," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2017, p. 9, doi: 10.1109/IEDM.2017.8268357.

[19] J. Liu et al., "1.2 kV vertical GaN fin JFETs with robust avalanche and fast switching capabilities," *IEDM Tech. Dig.*, 2020, pp. 23.2.1–23.2.4, doi: 10.1109/IEDM13553.2020.9372048.

[20] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, "Vertical GaN-based trench gate metal oxide semiconductor field-effect transistors on GaN bulk substrates," *Appl. Phys. Exp.*, vol. 1, no. 1, Jan. 2008, Art. no. 011105, doi: 10.1143/apex.1.011105.

[21] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "1.8 mΩ·cm^2 vertical GaN-based trench metal–oxide–semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation," *Appl. Phys. Exp.*, vol. 8, no. 5, May 2015, Art. no. 054101, doi: 10.7567/apex.8.054101.

[22] R. Li, Y. Cao, M. Chen, and R. Chu, "600 V/ 1.7 Ω normally-off GaN vertical trench metal–oxide–semiconductor field-effect transistor," *IEEE Electron Device Lett.*, vol. 37, no. 11, pp. 1466–1469, Nov. 2016, doi: 10.1109/LED.2016.2614515.

[23] W. Li et al., "Development of GaN vertical trench-MOSFET with MBE regrown channel," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2558–2564, Jun. 2018, doi: 10.1109/TED.2018.2829125.

[24] C. Liu, R. Abdul Khadar, and E. Matioli, "GaN-on-Si quasi-vertical power MOSFETs," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 71–74, Jan. 2018, doi: 10.1109/LED.2017.2779445.

[25] R. Zhu, H. Jiang, C. W. Tang, and K. M. Lau, "Effects of p-GaN body doping concentration on the ON-state performance of vertical GaN trench MOSFETs," *IEEE Electron Device Lett.*, vol. 42, no. 7, pp. 970–973, Jul. 2021, doi: 10.1109/LED.2021.3080260.

[26] D. Ji et al., "Large-area in-situ oxide, GaN interlayer-based vertical trench MOSFET (OG-FET)," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 711–714, May 2018, doi: 10.1109/LED.2018.2813312.

[27] D. Favero et al., "Influence of drain and gate potential on gate failure in semi-vertical GaN-on-Si trench MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Dallas, TX, USA, Mar. 2022, pp. P20-1–P20-4, doi: 10.1109/IRPS48227.2022.9764600.

[28] N. Yamashita, N. Murakami, and T. Yachi, "Conduction power loss in MOSFET synchronous rectifier with parallel-connected Schottky barrier diode," *IEEE Trans. Power Electron.*, vol. 13, no. 4, pp. 667–673, Jul. 1998, doi: 10.1109/63.704135.

[29] T. Morita et al., "GaN gate injection transistor with integrated Si Schottky barrier diode for highly efficient DC–DC converters," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2012, pp. 7.2.1–7.2.4, doi: 10.1109/IEDM.2012.6478996.

[30] J. Zhang and J.-S. Lai, "A synchronous rectification featured soft-switching inverter using CoolMOS," in *Proc. APEC*, Dallas, TX, USA, Mar. 2006, pp. 810–815, doi: 10.1109/APEC.2006.1620632.

[31] C. Liu, R. A. Khadar, and E. Matioli, "Vertical GaN-on-Si MOSFETs with monolithically integrated freewheeling Schottky barrier diodes," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1034–1037, Jul. 2018, doi: 10.1109/LED.2018.2841959.

[32] J. Wei, M. Zhang, H. Jiang, X. Zhou, B. Li, and K. J. Chen, "Superjunction MOSFET with dual built-in Schottky diodes for fast reverse recovery: A numerical simulation study," *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1155–1158, Jul. 2019, doi: 10.1109/LED.2019.2917556.

[33] M. Zhang, J. Wei, X. Zhou, H. Jiang, B. Li, and K. J. Chen, "Simulation study of a power MOSFET with built-in channel diode for enhanced reverse recovery performance," *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 79–82, Jan. 2019, doi: 10.1109/LED.2018.2881234.

[34] S. Yang, S. Han, and K. Sheng, "Vertical GaN power rectifiers: interface effects and switching performance," *Appl. Phys. Lett.*, vol. 36, no. 2, Dec. 2020, Art. no. 024005, doi: 10.1088/1361-6641/abca0d.

[35] Z. Bian et al., "Leakage mechanism of quasi-vertical GaN Schottky barrier diodes with ultra-low turn-on voltage," *Appl. Phys. Exp.*, vol. 12, no. 8, Aug. 2019, Art. no. 084004, doi: 10.7567/1882-0786/ab3297.

[36] Y. Zhang et al., "Novel GaN trench MIS barrier Schottky rectifiers with implanted field rings," in *IEDM Tech. Dig.*, Dec. 2016, pp. 10.2.1–10.2.4, doi: 10.1109/IEDM.2016.7838386.

[37] J. Liu et al., "Surge current and avalanche ruggedness of 1.2-kV vertical GaN p-n diodes," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 10959–10964, Oct. 2021, doi: 10.1109/TPEL.2021.3067019.

[38] H. Wang, S. Chen, H. Chen, and C. Liu, "Comprehensive design and numerical study of GaN vertical MPS diodes towards alleviated electric field crowding and efficient carrier injection," *IEEE J. Electron Devices Soc.*, vol. 10, pp. 504–511, Jun. 2022, doi: 10.1109/JEDS.2022.3185618.

[39] M. Kang et al., "Body diode reliability of commercial SiC power MOSFETs," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct. 2019, pp. 416–419, doi: 10.1109/WiPDA46397.2019.8998940.

[40] A. Fayyaz, G. Romano, and A. Castellazzi, "Body diode reliability investigation of SiC power MOSFETs," *Microelectron. Rel.*, vol. 64, pp. 530–534, Sep. 2016, doi: 10.1016/j.microrel.2016.07.044.

[41] J. Park et al., "Control of pn-junction turn-on voltage in 4H-SiC merged PiN Schottky diode," *Appl. Phys. Lett.*, vol. 110, no. 14, pp. 1–5, Apr. 2017, doi: 10.1063/1.4979790.

[42] K. Dannecker and J. Baringhaus, "Design and simulation of gallium nitride trench MOSFETs for applications with high lifetime demand," *J. Comput. Electron.*, vol. 20, no. 5, pp. 1685–1693, Jul. 2021, doi: 10.1007/s10825-021-01736-1.

[43] S. Han, S. Yang, and K. Sheng, "Fluorine-implanted termination for vertical GaN Schottky rectifier with high blocking voltage and low forward voltage drop," *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1040–1043, Jul. 2019, doi: 10.1109/LED.2019.2915578.